

LLW-1/LGG-1 Schematics

Sandy Bridge

Cougar Point

2011-01-18

REV : -1

DY:None Installed

UMA:UMA platform installed only

PX:Discrete(both Robson and Whistler) SKU installed

RBS:Robson SKU installed only

WTL:Whistler SKU installed only

SAMSUNG:Use SAMSUNG VRAM

Hynix:Use Hynix VRAM

VRAM_1G:Use 1G VRAM

VRAM_2G:Use 2G VRAM

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size

A3

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Tuesday, January 18, 2011

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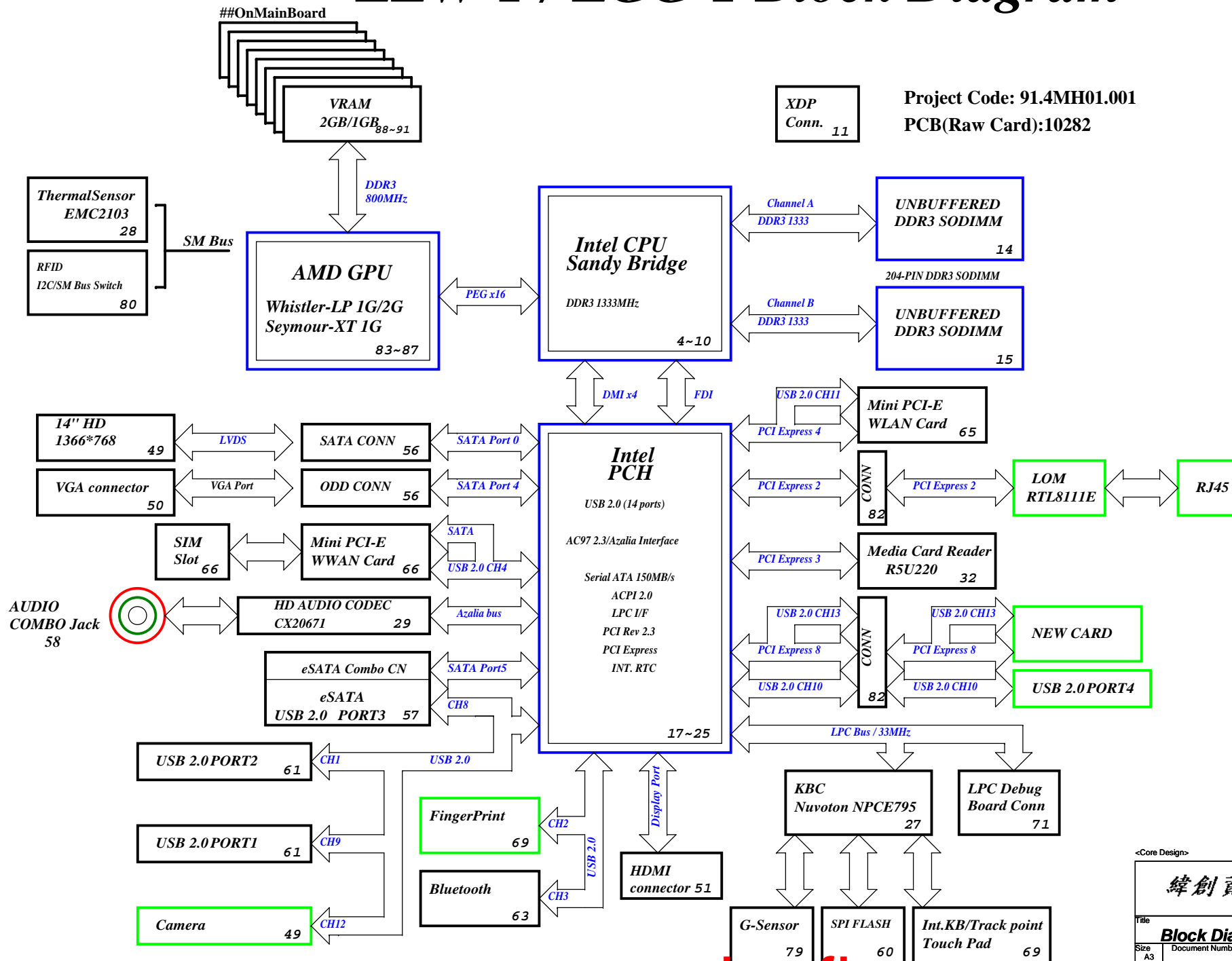
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LLW-1 / LGG-1

LLW-1 / LGG-1 Block Diagram



PCB Layer Stackup			
L1: TOP	L5: VCC		
L2: GND	L6: Signal		
L3: Signal	L7: GND		
L4: Signal	L8: BOTTOM		
Battery Charger/Selector			
BQ24745	40		
INPUTS		OUTPUTS	
DCBATOUT		BT+	
System DC/DC			
BD95280	41		
PWR_3D3V_DCBATOUT	3D3V_S5		
PWR_5V_DCBATOUT	5V_S5		
CPU DC/DC			
NCP6131	42~44		
DCBATOUT	VCC_CORE		
DCBATOUT_VCC_GFXCORE	VCC_GFXCORE		
ID05V_VTT			
TPS51218	45		
PWR_ID05V_DCBATOUT	ID05V_VTT		
ID5V_S3			
TPS51218	46		
PWR_ID5V_DCBATOUT	ID5V_S3		
ID75V			
RT9026	46		
ID5V_S3	DDR_VREF_S3		
	ID75V_S0		
ID8V_S0			
RT8015	47		
3D3V_S5	ID8V_S0		
VCCSA			
RT8208B	48		
PWR_VCCSA_DCBATOUT	ID85V_S0		
GFX CORE			
RT8208B	92		
PWR_DCBATOUT_VGA_CORE	VGA_CORE		
IV_VGA			
RT9025	93		
ID5V_S3	IV_VGA_S0		
ID8V_VGA			
RT9025	93		
3D3V_S5	ID8V_VGA_S0		

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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

PCIE Routing

LANE1	RESERVED
LANE2	LAN
LANE3	CARD READER
LANE4	MiniCard WLAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	RESERVED
LANE8	NEW CARD

SATA Table

SATA	
Pair	Device
0	HDD
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

Pair	Device
0	X
1	USB2
2	FINGERPRINT
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	X
6	X
7	X
8	ESATA1
9	USB1
10	USB Ext. port 4
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_SFPCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		Ref Des	HURON RIVER ORB
Device	Address	Hex	Bus
EC SMBus 1 Battery Capacity Board			KBC_SDA1/KBC_SCL1 KBC_SDA1/KBC_SCL1
EC SMBus 2 PCH MXM LCD Thermal Sensor			KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2
PCH SMBus CK505 Clock Generator SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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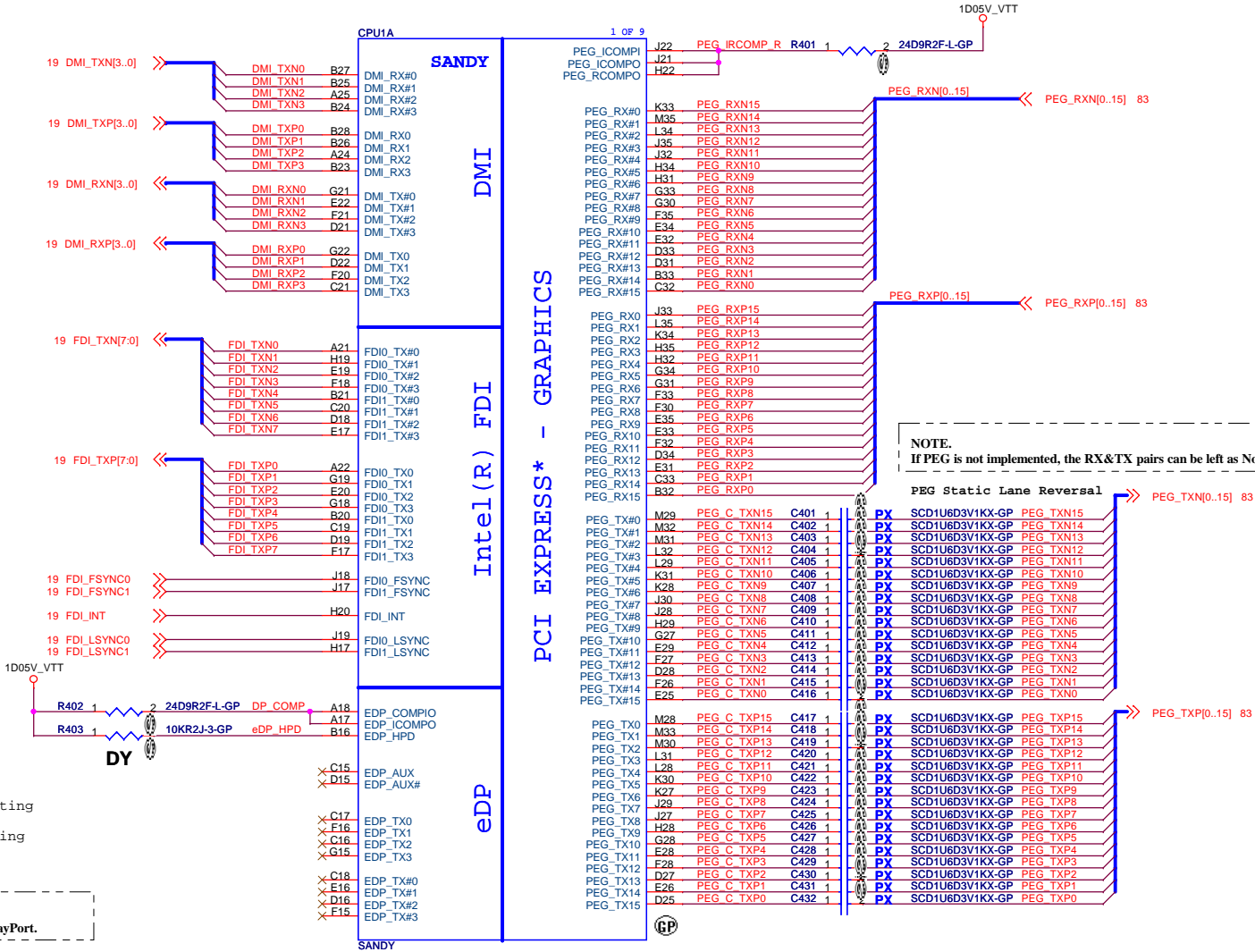
Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

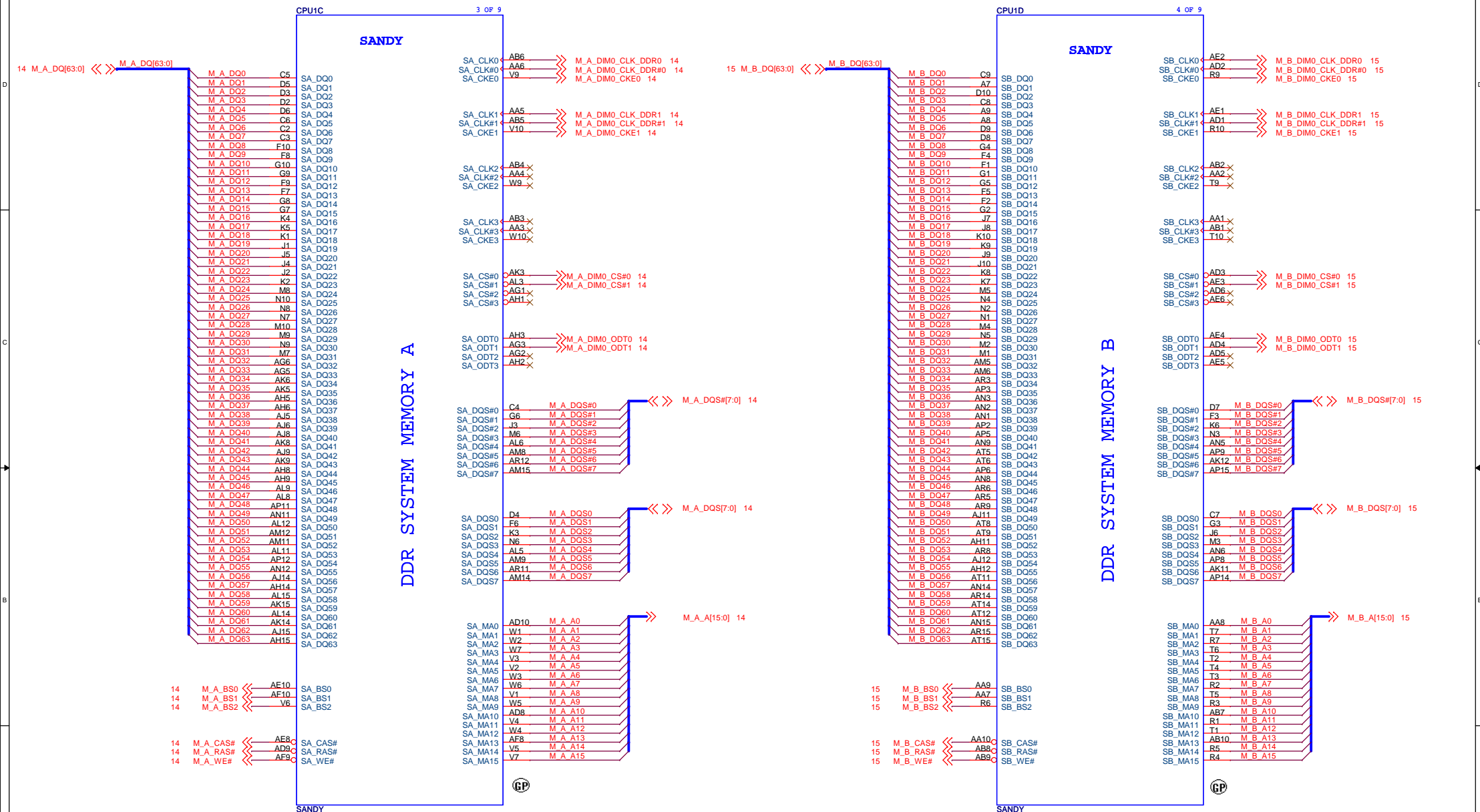
Note:
Lane reversal does not apply to
FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing
length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing
length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.



SSID = CPU



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CPU (DDR)

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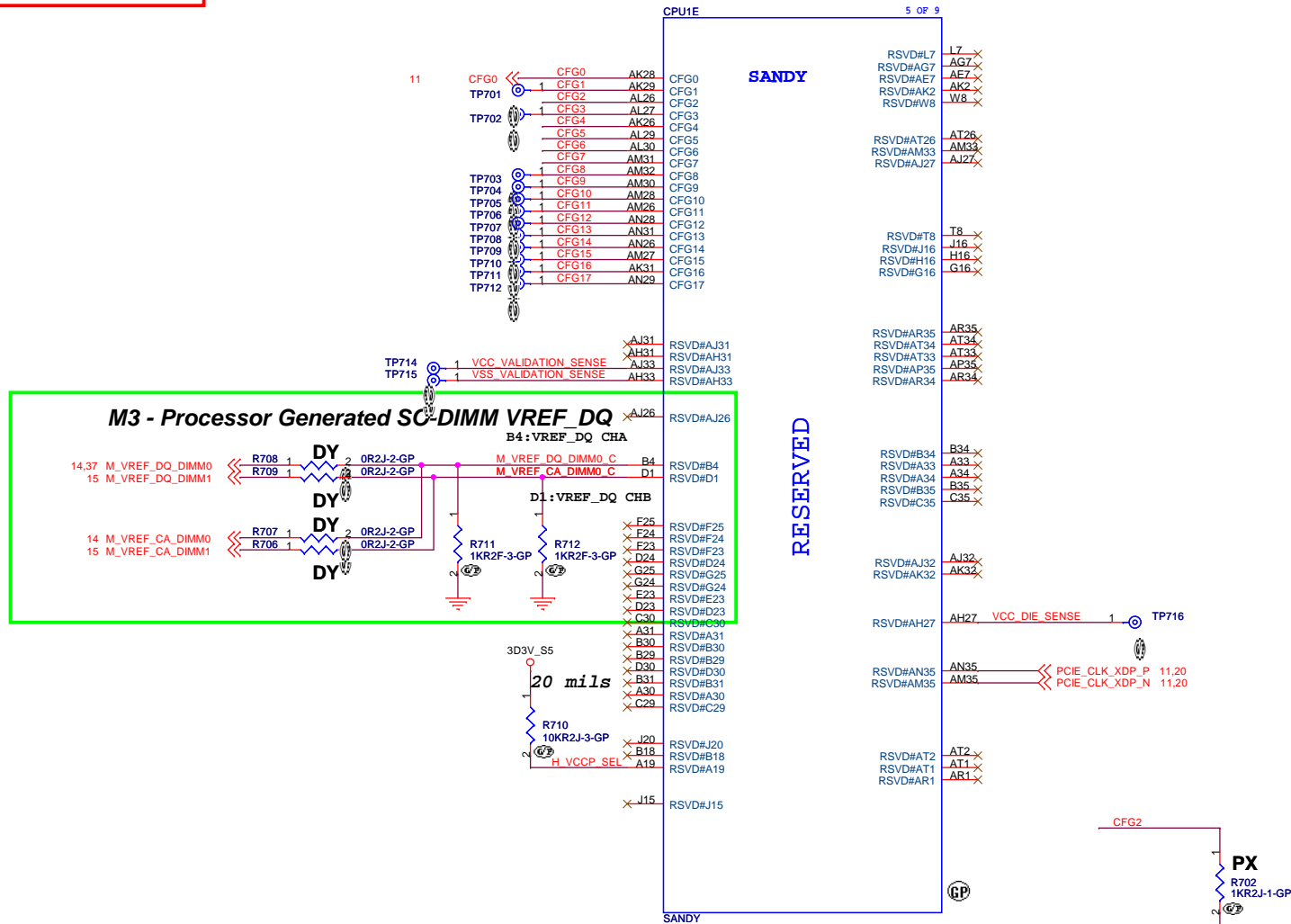
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SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

SSID = CPU

POWER

PROCESSOR CORE POWER

53A

VCC_CORE

SANDY

VCC_CORE

POWER

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VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

CORE SUPPLY

SVID

SENSE LINES

SANDY

VIDALERT# A/J29 H_CPU_SVIDALRT# R803 1 2 43R2J-GP VR_SVID_ALERT# 42
VIDCLK A/J30 H_CPU_SVIDCLK R803 1 2 43R2J-GP H_CPU_SVIDCLK 42
VIDSOUT A/J28 H_CPU_SVIDDAT R803 1 2 43R2J-GP H_CPU_SVIDDAT 42

R801, R802 need to close to CPU

VCC_CORE

R801 100R2F-L1-GP-U

R802 100R2F-L1-GP-U

VCC_SENSE

VSS_SENSE

VCCIO_SENSE

VSSIO_SENSE

VCCSENSE 42
VSSSENSE 42

VCCIO_SENSE 45
VSSIO_SENSE 45

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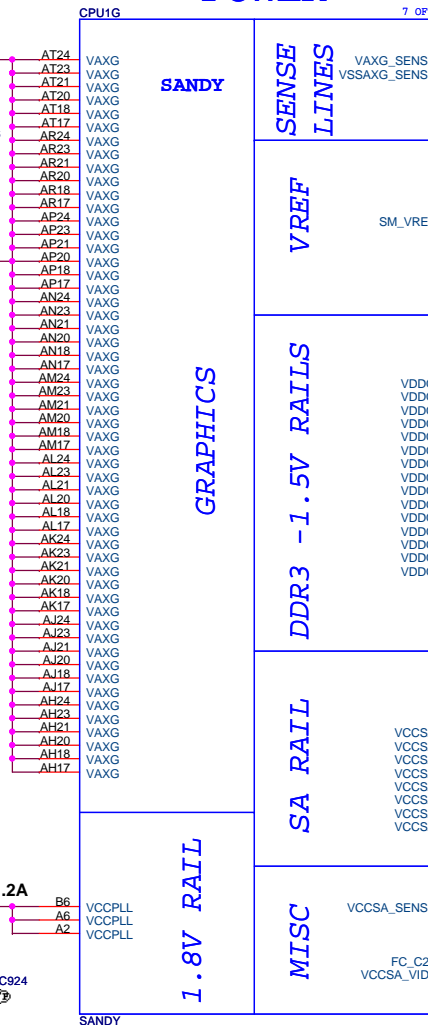
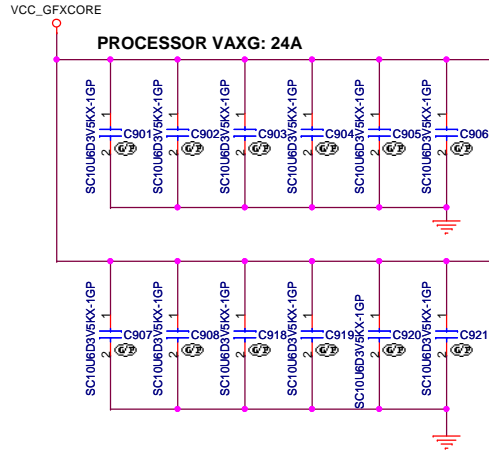
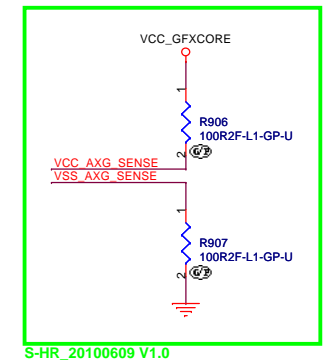
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Size Custom Document Number LLW-1 / LGG-1
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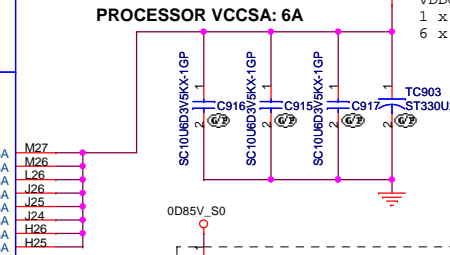
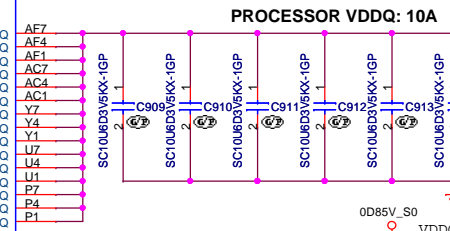
VAXG Output Decoupling Recommendation:
 2 x 470 uF at Bottom Socket Edge
 2 x 22 uF at Top Socket Cavity
 4 x 22 uF at Top Socket Edge
 2 x 22 uF at Bottom Socket Cavity
 4 x 22 uF at Bottom Socket Edge

R906, R907 close to CPU



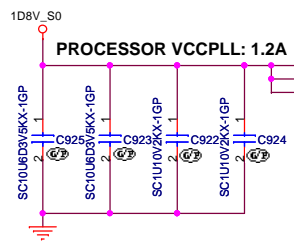
VAXG_SENSE 42
 VSSAXG_SENSE 42
 Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.
 +V_SM_VREF_CNT should have 10 mil trace width
 +V_SM_VREF_CNT 37

Routing Guideline:
 Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.



VDDQ Output Decoupling Recommendation:
 1 x 330 uF
 6 x 10 uF
 VCCSA Output Decoupling Recommendation:
 1 x 330 uF
 2 x 10 uF at Bottom Socket Cavity
 1 x 10 uF at Bottom Socket Edge

R902 need be close to pin H23.
 R902 10R2J-2-GP

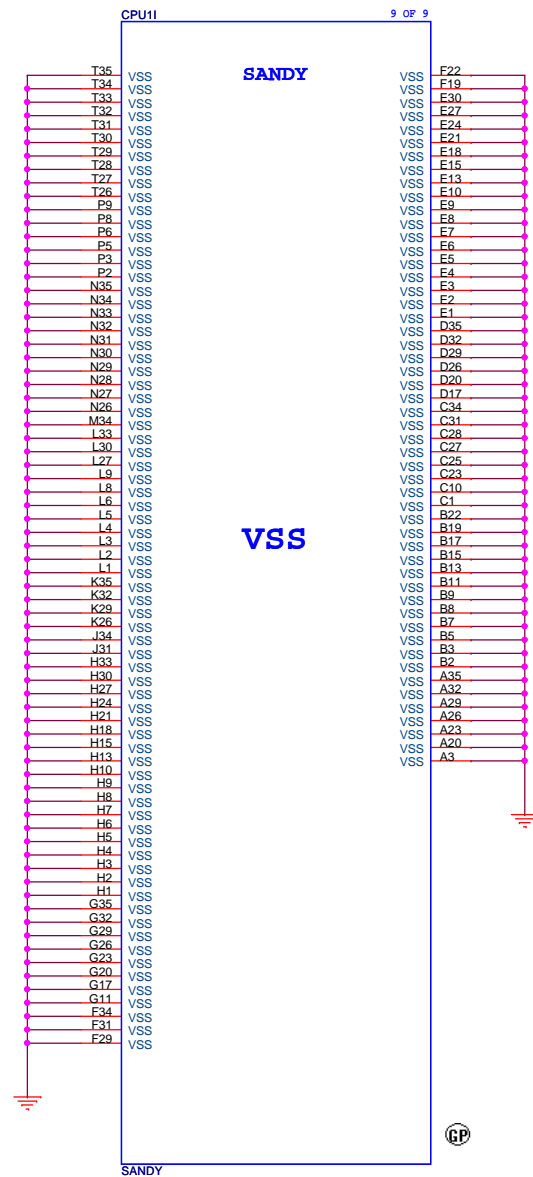
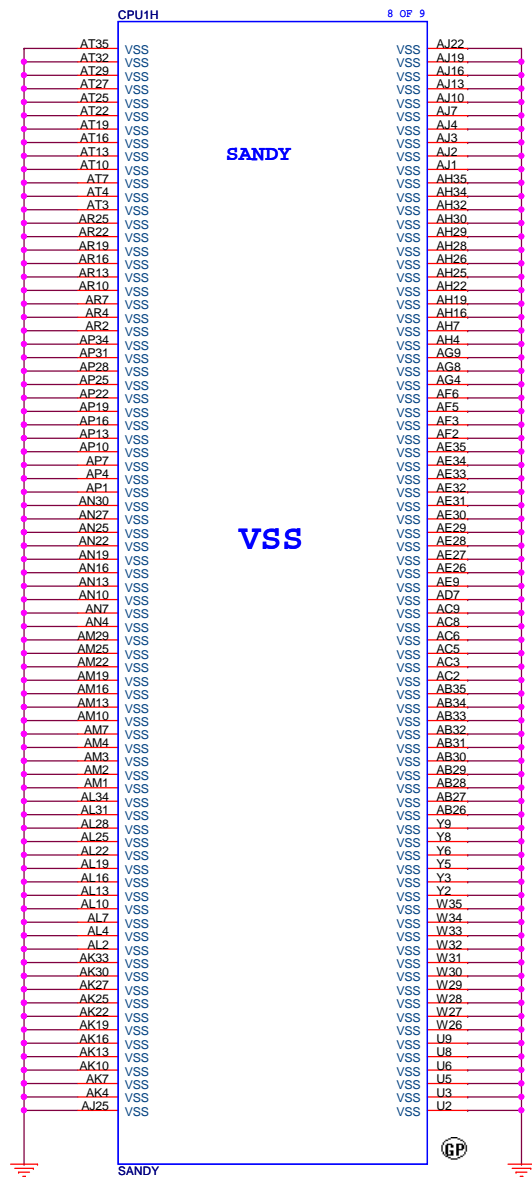


VCCPLL Output Decoupling Recommendation:
 1 x 330 uF
 2 x 1 uF
 1 x 10 uF

Disabling Guidelines for External Graphics Designs:
 Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
 Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

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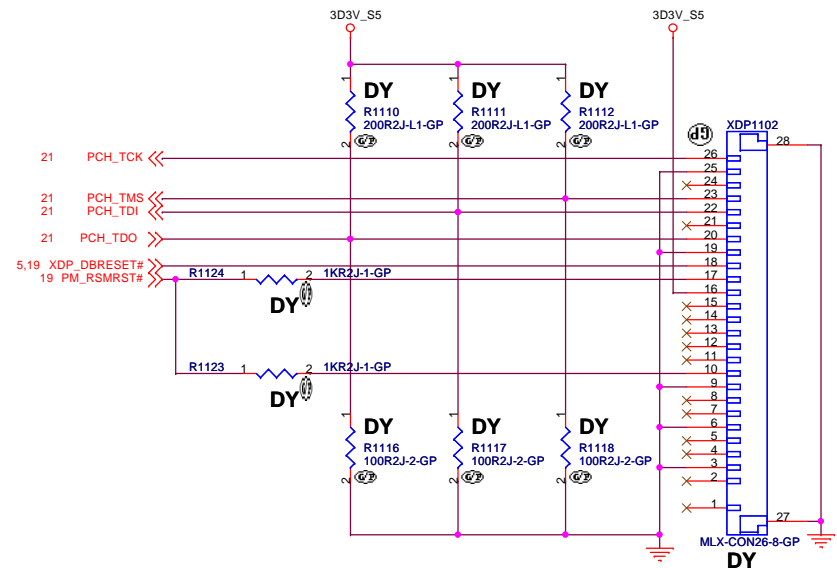
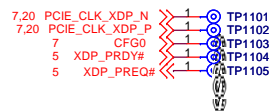
SSID = CPU



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DEBUG Interface for Processor.

CPU XDP SFF 26pin IF
 Pin 1 OBSFN_A0 (PREQ#, I/O)
 Pin 2 OBSFN_A1 (PRDY#, I/O)
 Pin 3 GND
 Pin 4 OBSDATA_A0 (Open, I/O)
 Pin 5 OBSDATA_A1 (Open, I/O)
 Pin 6 GND
 Pin 7 OBSDATA_A2 (Open, I/O)
 Pin 8 OBSDATA_A3 (Open, I/O)
 Pin 9 GND
 Pin 10 HOOK0 (PWRGD, In)
 Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
 Pin 12 HOOK2 (CFG0, Out)
 Pin 13 HOOK3 (vr_READYSYS_PWROK, Out)
 Pin 14 HOOK4 (BCLK, In)
 Pin 15 HOOK5 (BCLK#, In)
 Pin 16 VCCOBS_AB (VCCP Voltage of CPU, In)
 Pin 17 HOOK6 (RESET#, Out)
 Pin 18 HOOK7 (DBR#, Out)
 Pin 19 GND
 Pin 20 TDO, In
 Pin 21 TRST#, Out
 Pin 22 TDI, Out
 Pin 23 TMS, Out
 Pin 24 TCK1 (Open)
 Pin 25 GND
 Pin 26 TCK0 ,Out

TABLE

PCH PIN	REF DES	PCH ES1 JTAG		PCH ES2 JTAG		PRODUCTION	
		Enable	Disable	Enable	Disable	Enable	Disable
TDO	R1110	DY	DY	200 Ohms	DY	DY	DY
	R1116	DY	DY	100 Ohms	DY	DY	DY
	R2	DY	DY	DY	DY	51 Ohms	DY
TMS	R1112	200 Ohms	DY	200 Ohms	DY	DY	DY
	R1118	100 Ohms	DY	100 Ohms	DY	DY	DY
	R91	DY	DY	DY	DY	51 Ohms	DY
TDI	R1111	200 Ohms	20K Ohms	200 Ohms	DY	DY	DY
	R1117	100 Ohms	10K Ohms	100 Ohms	DY	DY	DY
	R90	DY	DY	DY	DY	51 Ohms	DY
TCK	R541	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms
TRST#	R953	20K Ohms	DY	DY	DY	DY	DY
	R535	10K Ohms	DY	DY	DY	DY	DY
	R103	DY	DY	DY	DY	DY	DY

DEBUG Interface for PCH.

PCH XDP SFF 26pin IF
 Pin 1 OBSFN_A0 (Open, I/O)
 Pin 2 OBSFN_A1 (Open, I/O)
 Pin 3 GND
 Pin 4 OBSDATA_A0 (Open, I/O)
 Pin 5 OBSDATA_A1 (Open, I/O)
 Pin 6 GND
 Pin 7 OBSDATA_A2 (Open, I/O)
 Pin 8 OBSDATA_A3 (Open, I/O)
 Pin 9 GND
 Pin 10 HOOK0 (RSMRST#, In)
 Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
 Pin 12 HOOK2 (Open)
 Pin 13 HOOK3 (Open)
 Pin 14 HOOK4 (Open)
 Pin 15 HOOK5 (Open)
 Pin 16 VCCOBS_AB (3.3VSUS, In)
 Pin 17 HOOK6 (RSMRST#, Out)
 Pin 18 HOOK7 (DBR#, Out)
 Pin 19 GND
 Pin 20 TDO (JTAG, In)
 Pin 21 TRST# (Open)
 Pin 22 TDI (JTAG, Out)
 Pin 23 TMS (JTAG, Out)
 Pin 24 TCK1 (Open)
 Pin 25 GND
 Pin 26 TCK0 (JTAG, Out)

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CLOCK GEN

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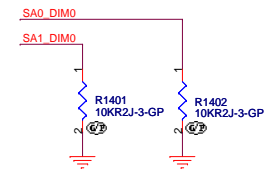
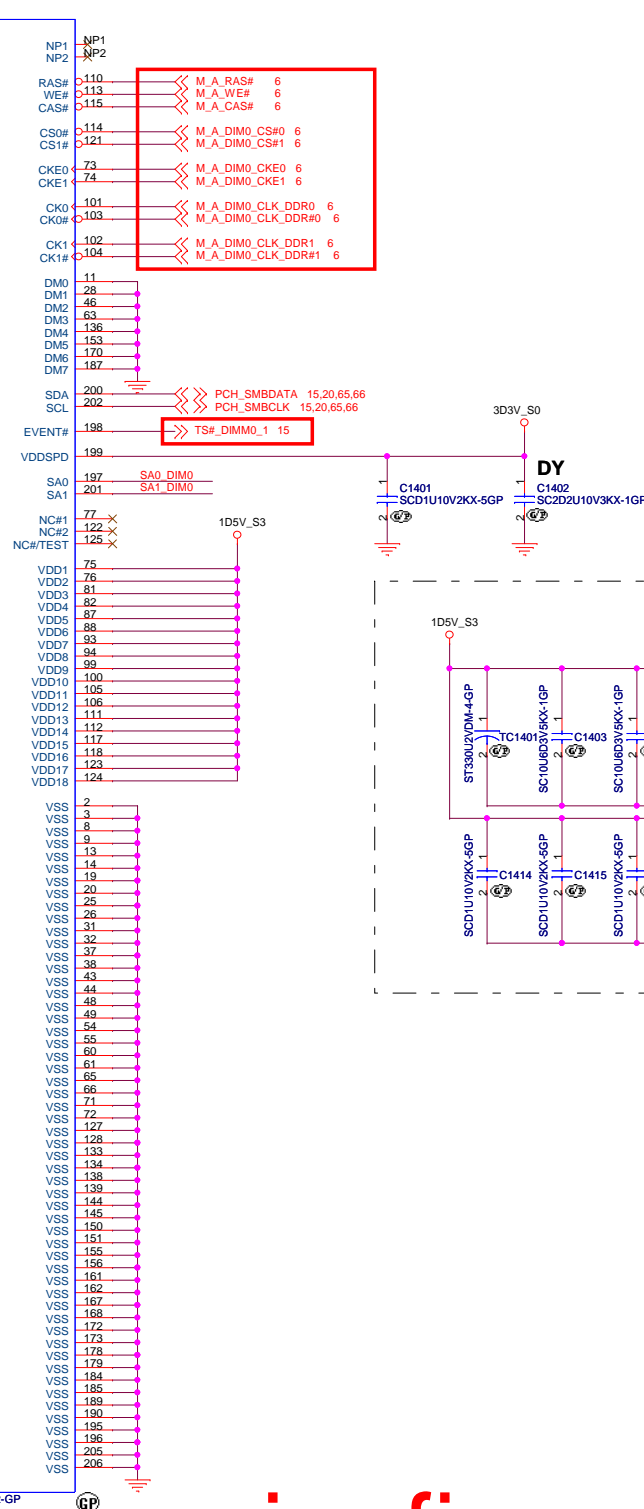
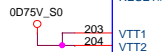
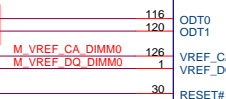
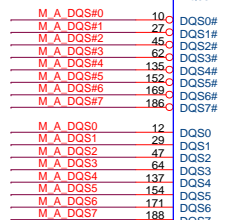
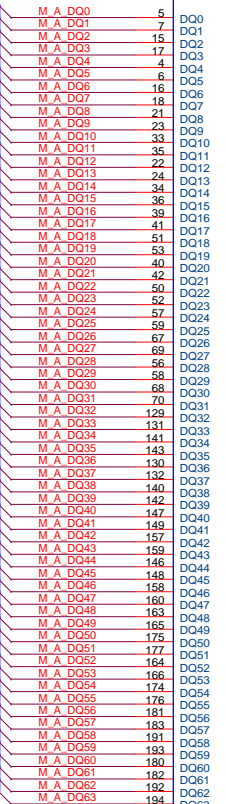
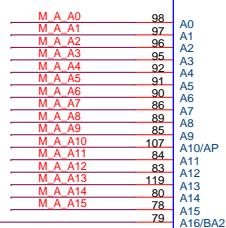
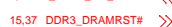
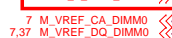
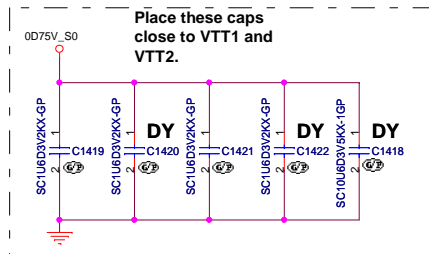
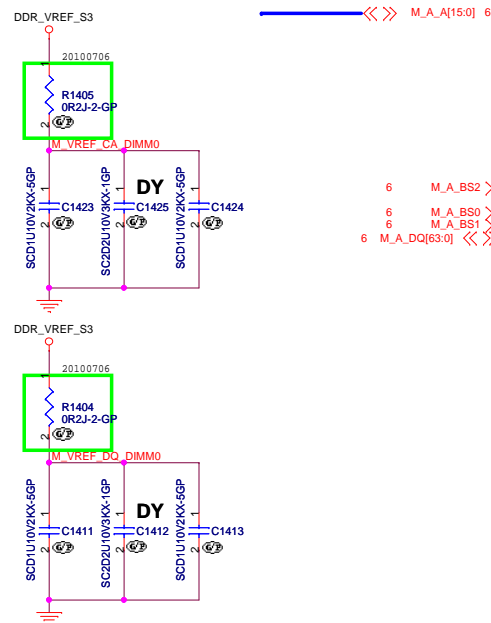
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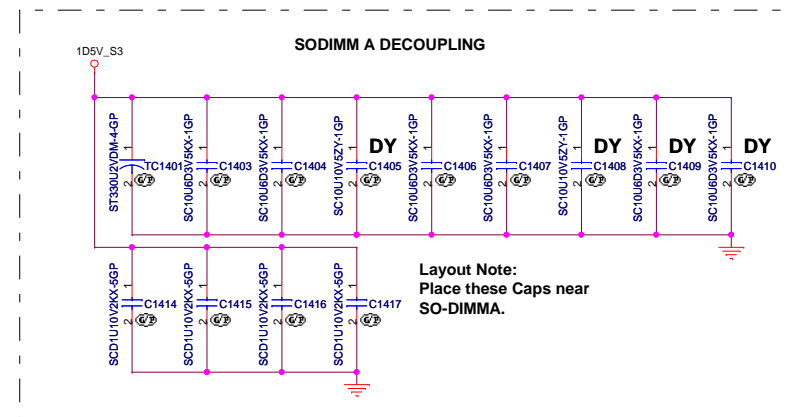
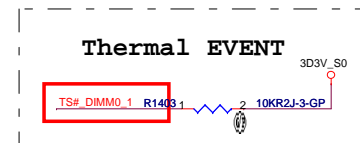
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SSID = MEMORY



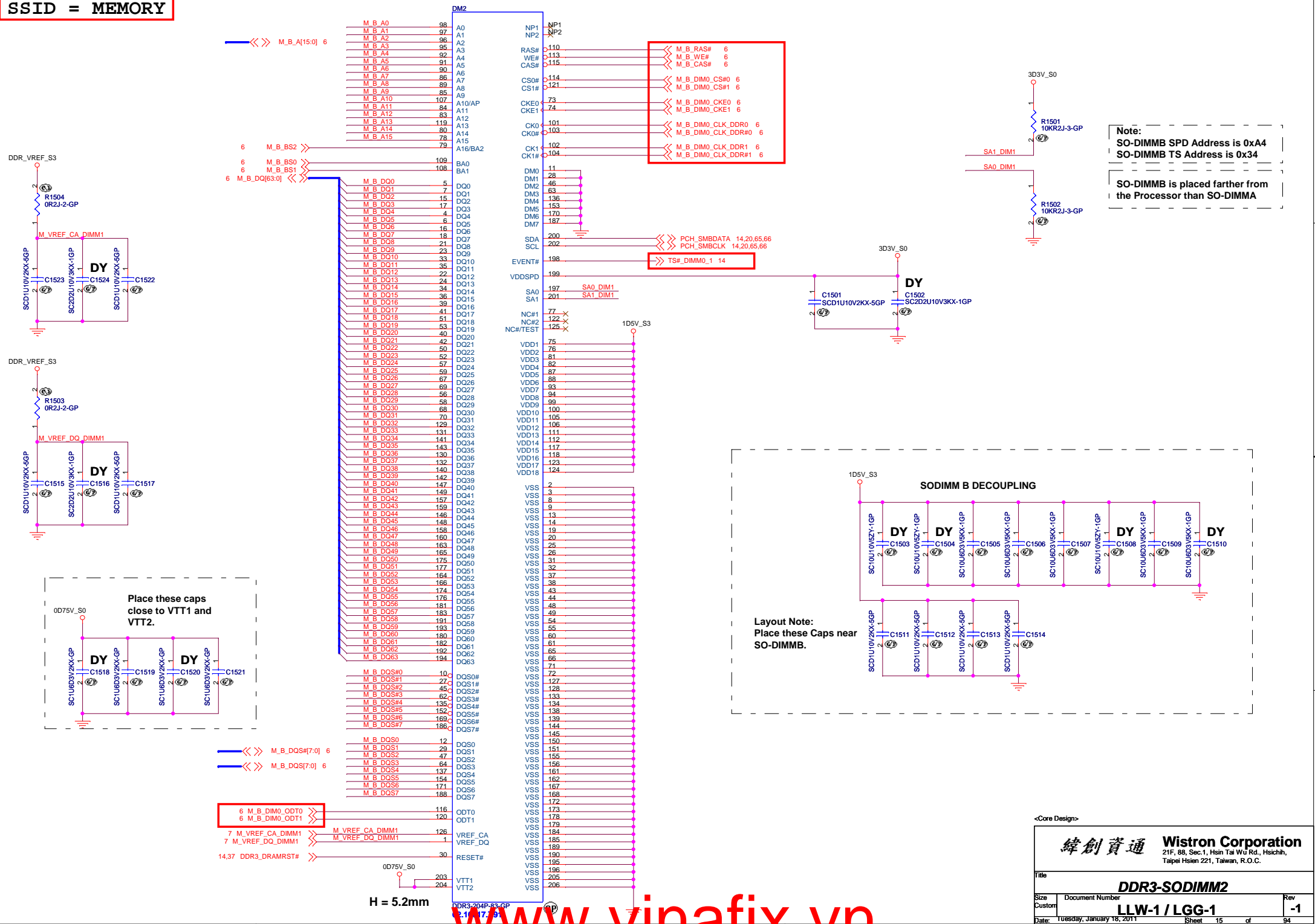
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



Layout Note:
Place these Caps near
SO-DIMMA.

SSID = MEMORY



(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR3-SODIMM2

Size
A4

Document Number

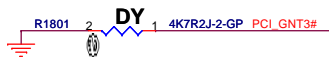
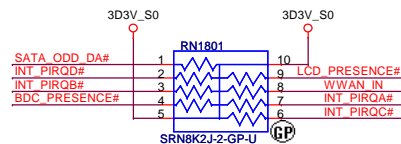
LLW-1 / LGG-1

Rev
-1

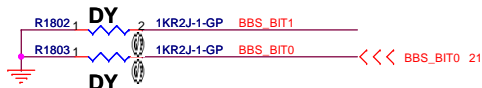
Date: Tuesday, January 18, 2011

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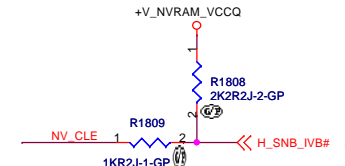
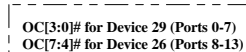
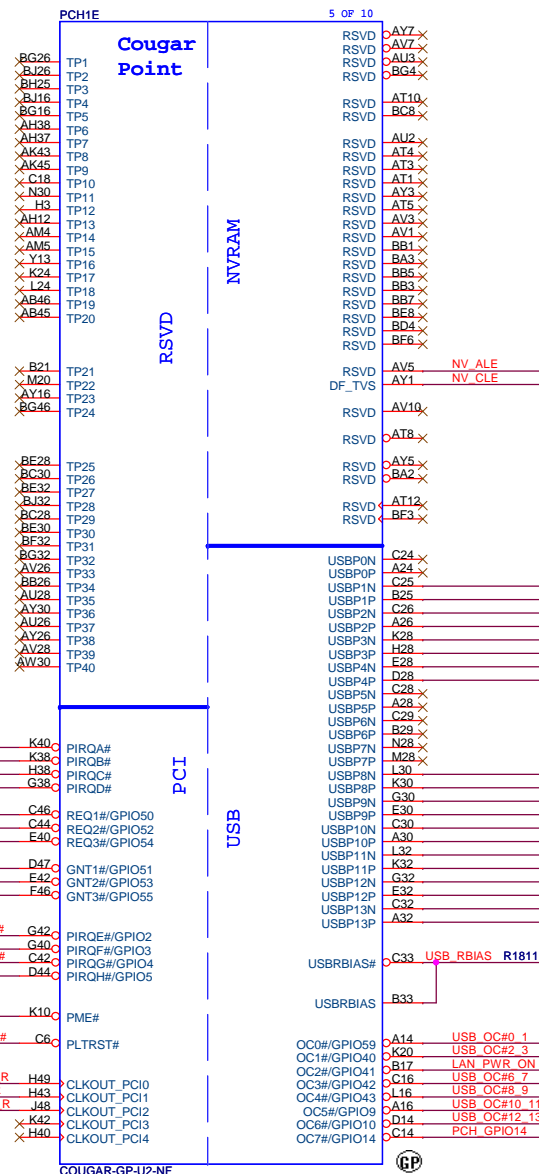
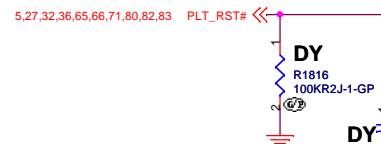
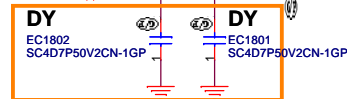
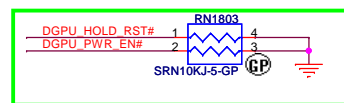
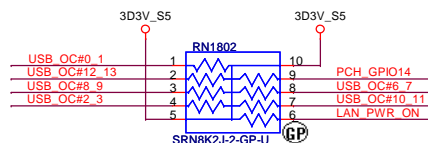
SSID = PCH



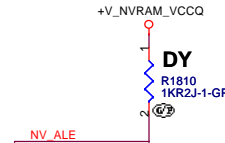
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



```
Danbury Technology:
Disabled when Low.
Enable when High.
```

USB	
Pair	Device
0	X
1	USB2
2	FINGERPRINT
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	X
6	X
7	X
8	ESATA1
9	USB1
10	USB Ext. port 4
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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Title			
PCH (PCI/USB/NVRAM)			
Size A3	Document Number LLW-1 / LGG-1		Rev -1
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SSID = PCH

4 DMI_RXN[3..0] <<>>=
4 DMI_RXP[3..0] <<>>=
4 DMI_TXN[3..0] <<>>=
4 DMI_TXP[3..0] <<>>=

FDI_TXN[7..0] 4
FDI_TXP[7..0] 4

Deep S4/S5 Supported

Deep S4/S5 **Not** Supported

VccDSW3_3

DPWROK

VccSUS3_3

RSMRST#

For platforms not supporting Deep S4/S5

- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSWRDNACK/GPIO30

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.

PCH1C

3 OF 10

**Cougar
Point**

DMI

FDI

System Power Management

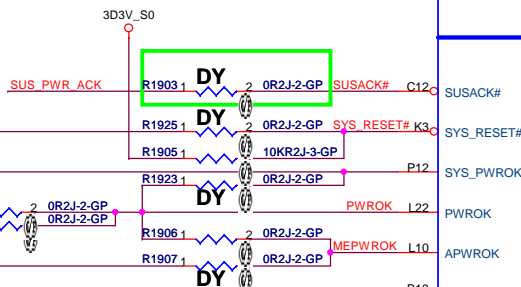
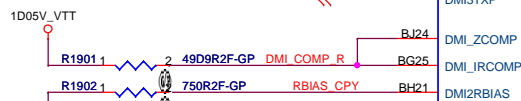
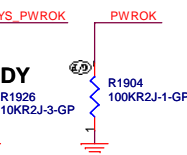
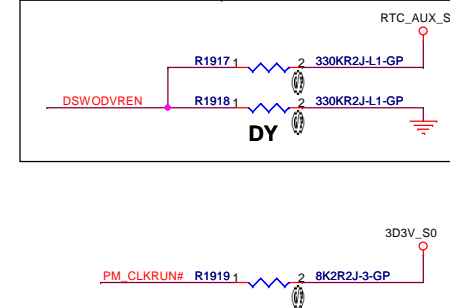
COUGAR-GP-U2-NF

FDI_RXN0 BJ14 <<>> FDI_TXN7 4
FDI_RXN1 AY14 <<>> FDI_TXN6 4
FDI_RXN2 BE14 <<>> FDI_TXN5 4
FDI_RXN3 BH13 <<>> FDI_TXN4 4
FDI_RXN4 BC12 <<>> FDI_TXN3 4
FDI_RXN5 BJ12 <<>> FDI_TXN2 4
FDI_RXN6 BG10 <<>> FDI_TXN1 4
FDI_RXN7 BG9 <<>> FDI_TXN0 4
FDI_RXP0 BJ14 <<>> FDI_TXP7 4
FDI_RXP1 BB14 <<>> FDI_TXP6 4
FDI_RXP2 BE14 <<>> FDI_TXP5 4
FDI_RXP3 BG13 <<>> FDI_TXP4 4
FDI_RXP4 BE12 <<>> FDI_TXP3 4
FDI_RXP5 BG12 <<>> FDI_TXP2 4
FDI_RXP6 BJ10 <<>> FDI_TXP1 4
FDI_RXP7 BH9 <<>> FDI_TXP0 4

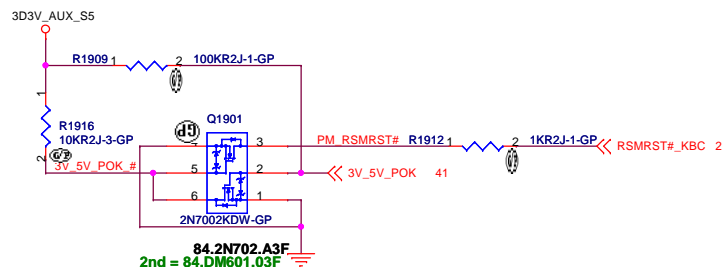
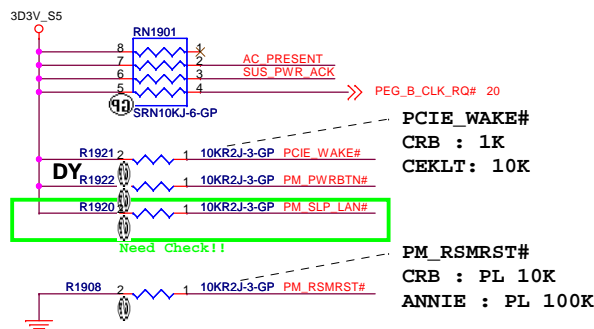
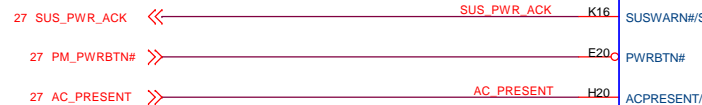
FDI_INT AW16 <<>> FDI_INT 4
FDI_FSYNCO AV12 <<>> FDI_FSYNCO 4
FDI_FSYNC1 BC10 <<>> FDI_FSYNC1 4
FDI_LSYNCO AV14 <<>> FDI_LSYNCO 4
FDI_LSYNC1 BB10 <<>> FDI_LSYNC1 4

DSWVRMEN A18 DSWODVREN
DPWROK E22 PCH DPWROK R1911 1 10KR2J-3-GP PM RSMRST#
WAKE# B9 PCIE_WAKE# <<>> PCIE_WAKE# 65,52
CLKRUN#/GPIO32 N3 PM_CLKRUN# <<>> PM_CLKRUN# 27
SUS_STAT#/GPIO61 G8 PM_SUS_STAT# 1 TP1901 TPAD14-GP
SUSCLK/GPIO62 N14 SUS_CLK R1913 1 0R2J-2-GP <<>> PCH_SUSCLK_KBC 27
SLP_S5#/GPIO63 D10 PM_SLP_S5# 1 TP1902 TPAD14-GP
SLP_S4# H4 SLP_S4# R R1914 1 0R2J-2-GP <<>> PM_SLP_S4# 27,46,82
SLP_S3# F4 SLP_S3# R R1915 1 0R2J-2-GP <<>> PM_SLP_S3# 27,36,37,47,82
SLP_A# G10 PM_SLP_A# 1 TP1903TPAD14-GP
SLP_SUS# G16 PM_SLP_SUS# 1 TP1904TPAD14-GP
PMSYNCH AP14 H_PM_SYNC <<>> H_PM_SYNC 5
SLP_LAN#/GPIO29 K14 PM_SLP_LAN# 1 TP1905TPAD14-GP

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



S0_PWR_GOOD after PM_SLP_S3# delay 200 ms



<Core Design>

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PCH (DMI/FDI/PM)		
Size A3	Document Number LLW-1 / LGG-1	Rev -1
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SSID = PCH

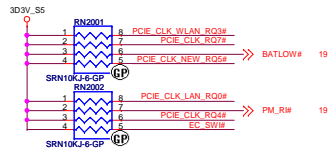
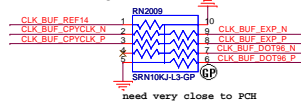
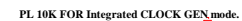
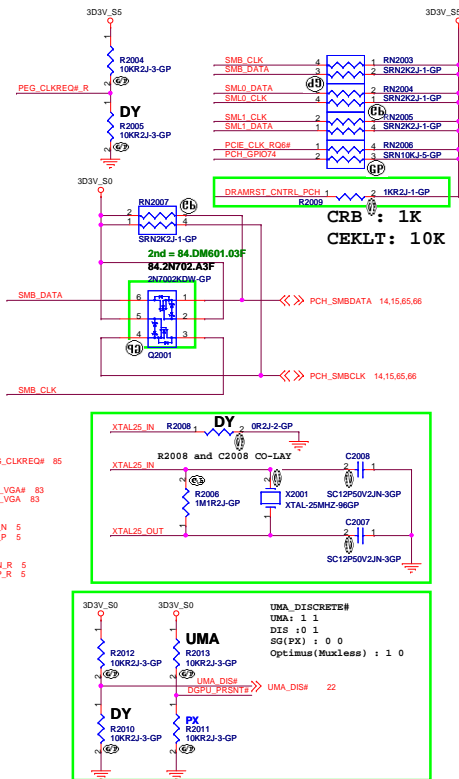
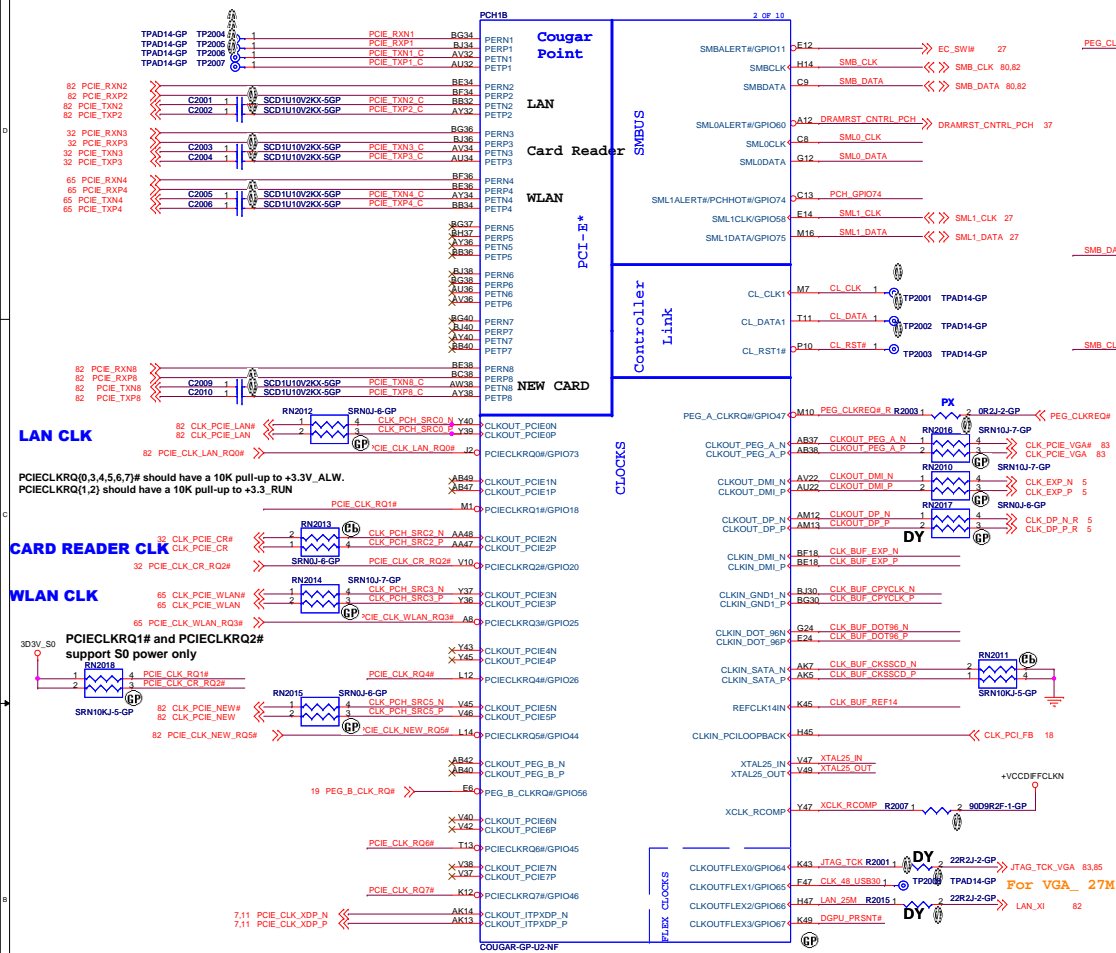


Table 20.1- Dual N-Channel MOSFET multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
PANJIT	2N7002KDW	N/A	84.2N702.A3
DIODES	DMN601DWK-7	N/A	84.DM601.03
NXP	2N7002BKS	N/A	84.2N702.E3

«Core Design:

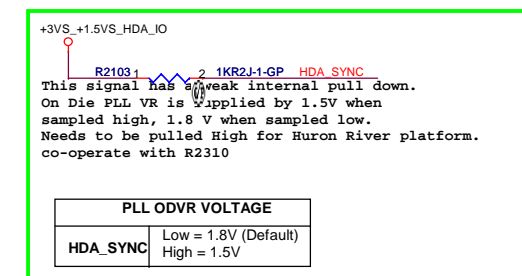
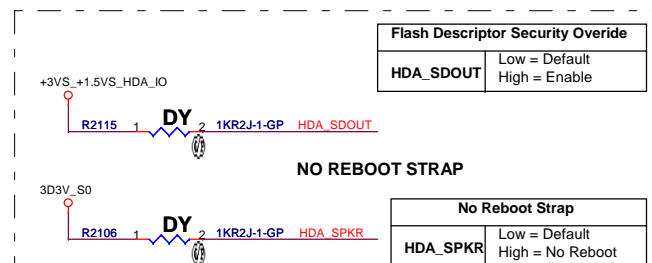
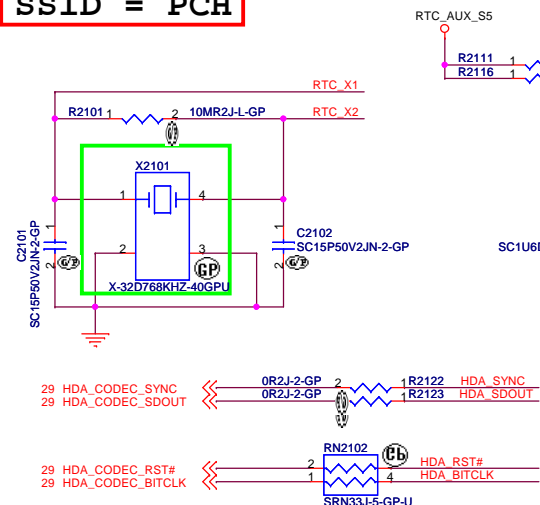
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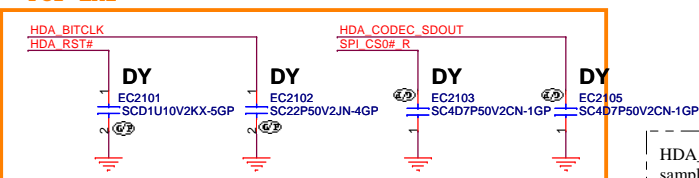
Title	PCH (PCI-E/SMBUS/CLOCK/CL)
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Size A2	Document Number LLW-1 / LGG-1	Rev -
Date: Tuesday, January 18, 2011	Sheet 20 of	94

SSID = PCH



For EMI

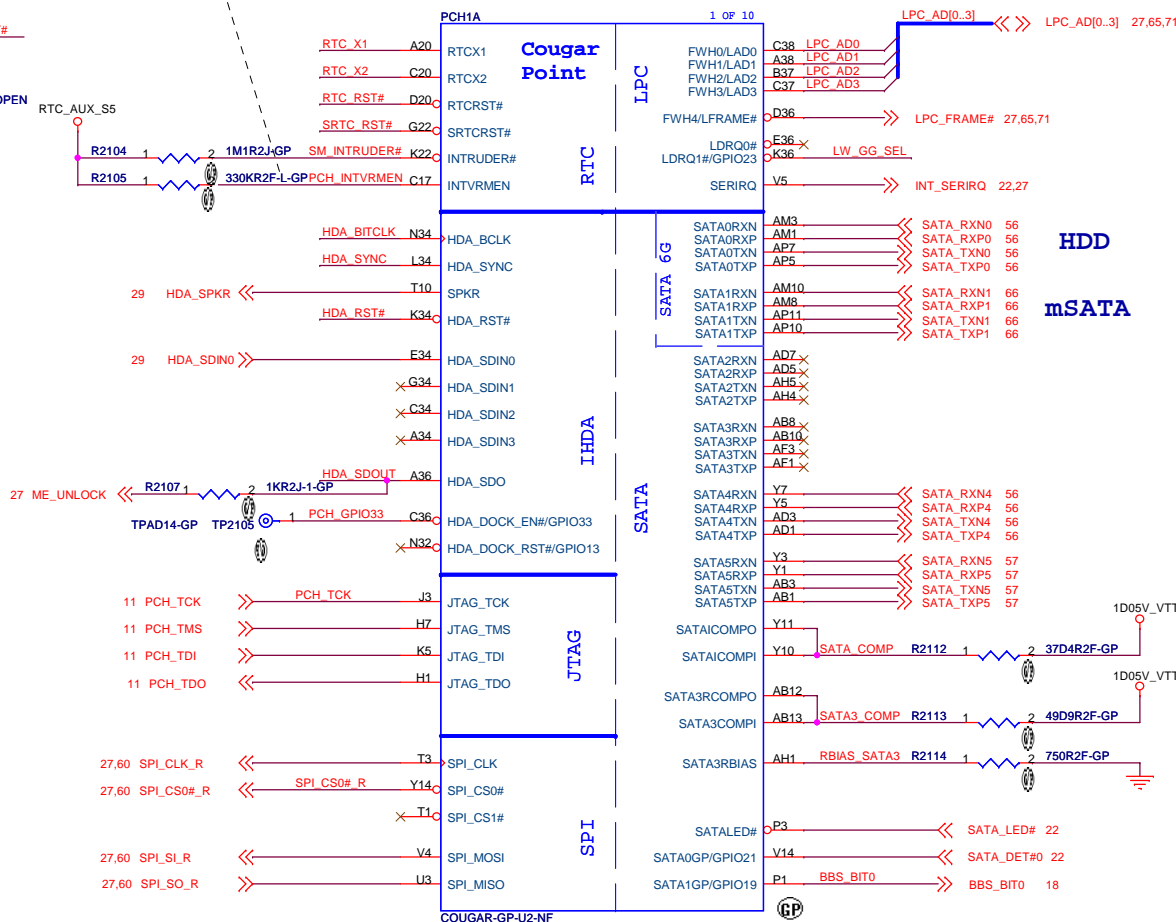
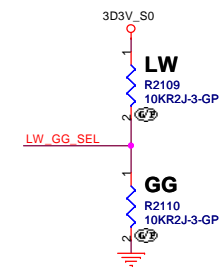


HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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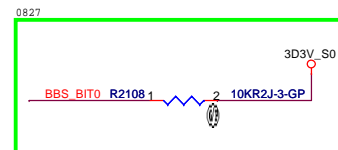
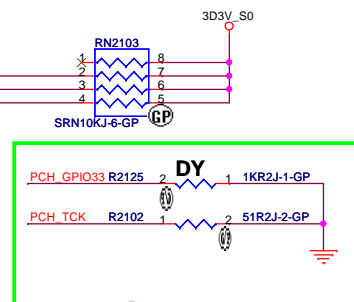
Table 21.1 Project_ID

	LW_GG_SEL
LW	High
GG	LOW



HDD
mSATA

ODD
ESATA



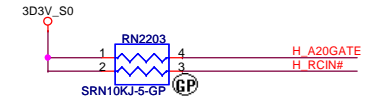
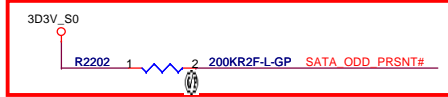
<Core Design>

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Title			
PCH (SPI/RTC/LPC/SATA/IHDA)			
Size	Document Number	Rev	
A3	LLW-1 / LGG-1	-1	
Date:	Tuesday, January 18, 2011	Sheet	21 of 94

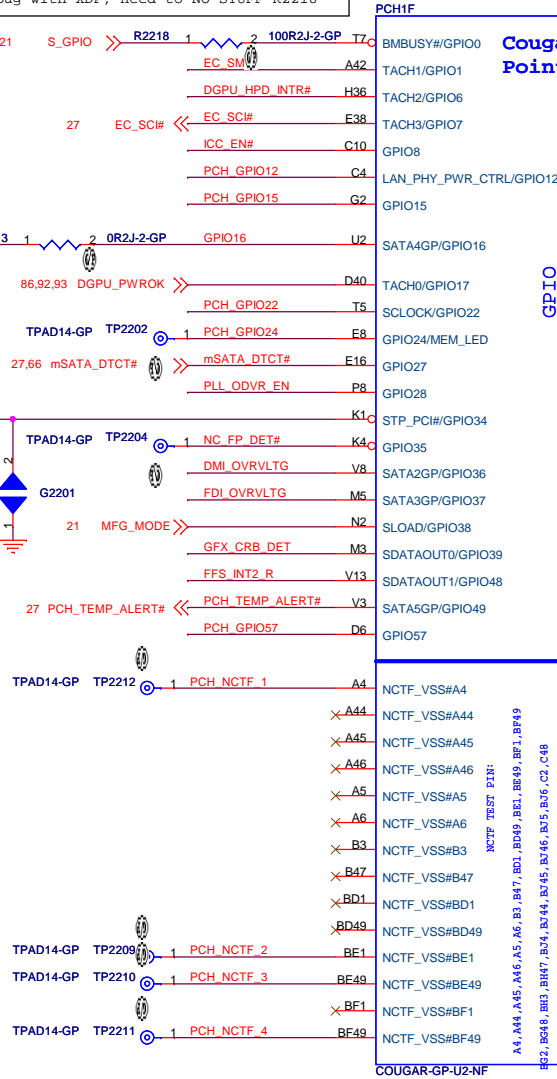
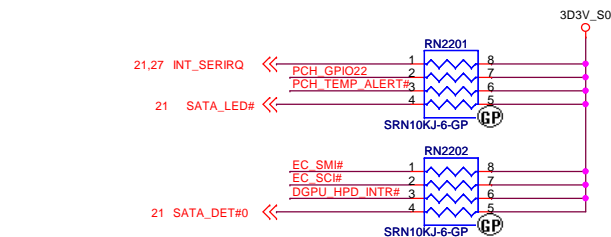
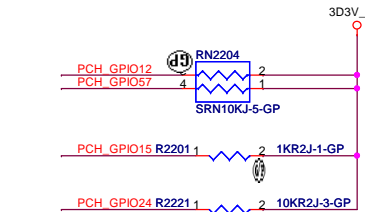
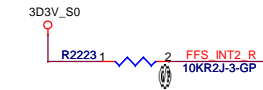
SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

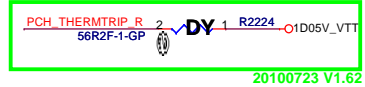
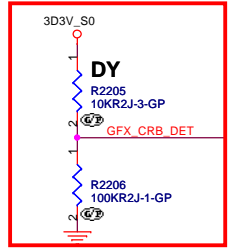
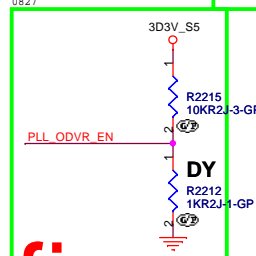
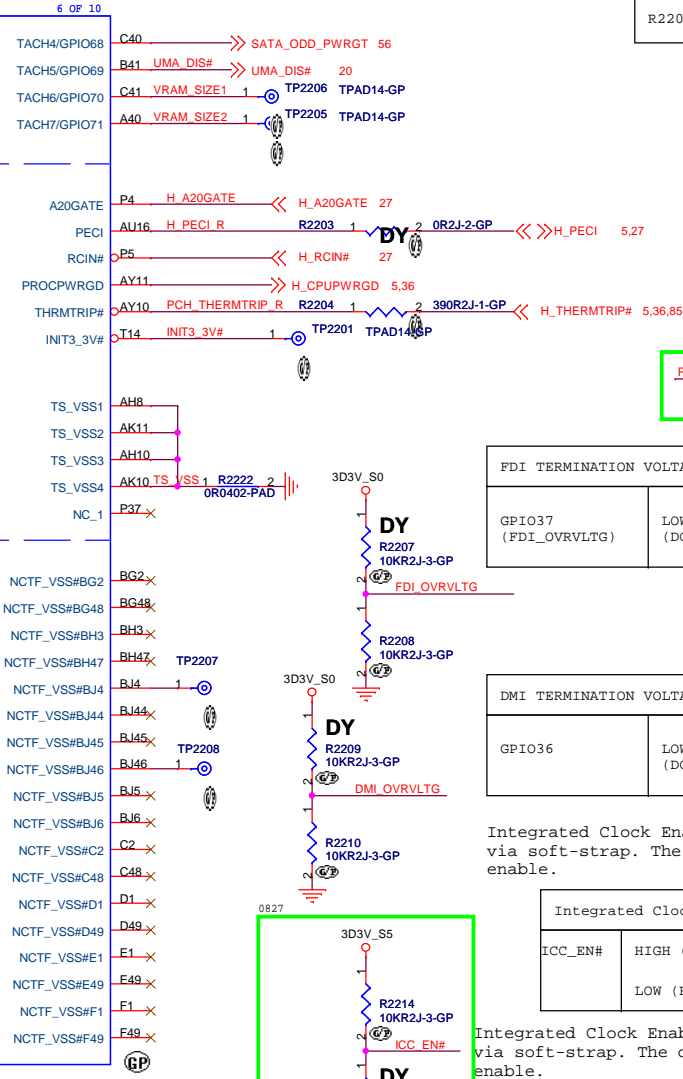


Cougar
Point

GPIO
CPU/MISC

NCTF

NCTF TEST PIN:
A4, A44, A45, A46, A5, A6, B3, B47, BE1, BE49, BF1, BF49
B37, B49, B83, BH7, B74, B744, B745, B746, C2, C48
D1, D49, E1, E49, F1, F49



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE	
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT	
DISABLED -- LOW (R2212 STUFFED)	

<Core Design>		
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Title PCH (GPIO/CPU)		
Size A3	Document Number LLW-1 / LGG-1	Rev -1
Date: Tuesday, January 18, 2011	Sheet 22 of 94	

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SSID = PCH

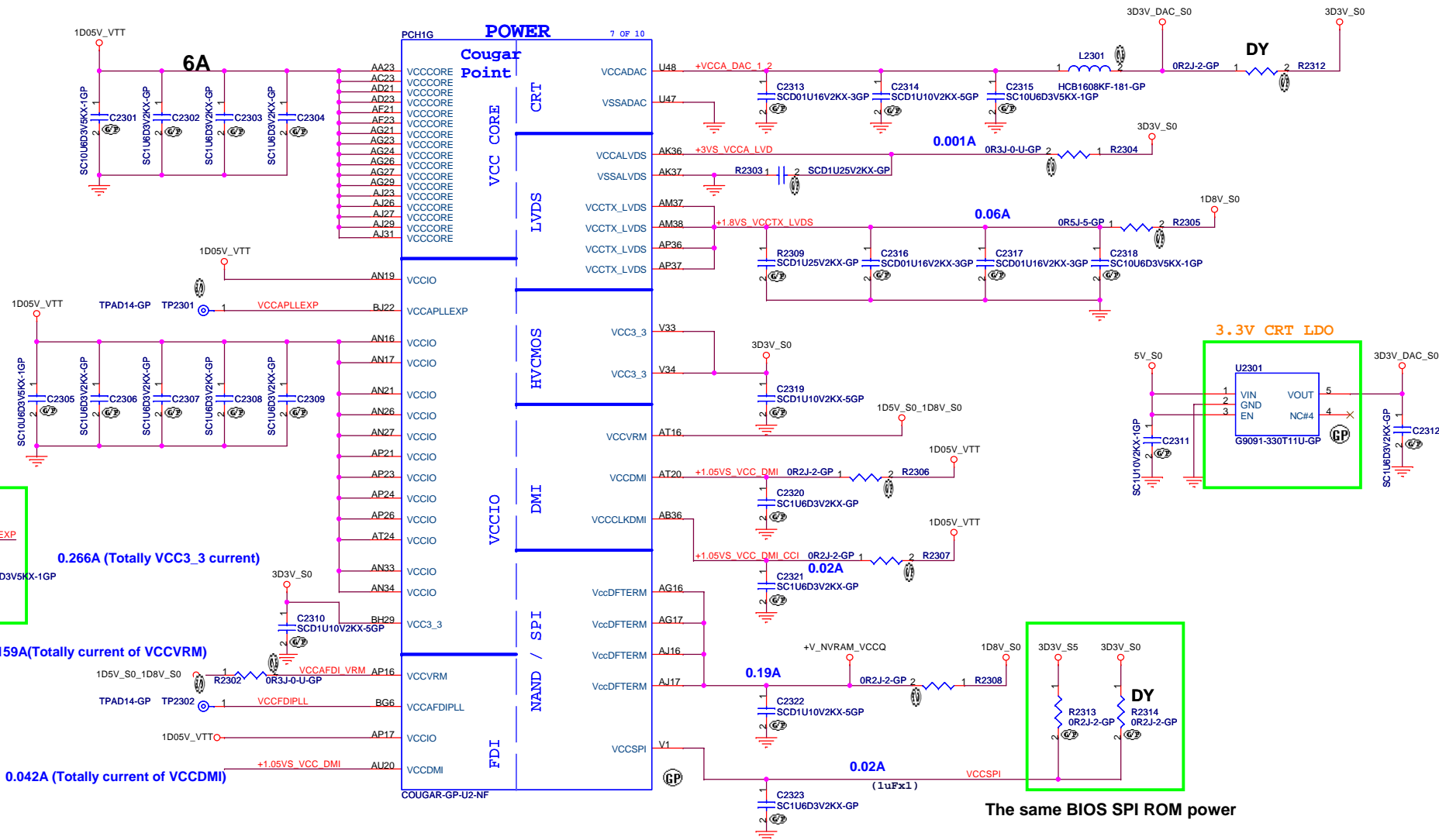


Table 23.1- LDO Regulator multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
GMT	G9091-330T11U	N/A	74.09091.J3F
RICHTEK	RT9198-33GBR	N/A	74.09198.Q7F

<Core Design>

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Title	Author	Date	Page
1. Introduction	John Doe	2023-10-27	10
2. Methodology	Jane Smith	2023-10-28	15
3. Results	Mike Johnson	2023-10-29	20
4. Discussion	Emily White	2023-10-30	25
5. Conclusion	David Brown	2023-10-31	30

PCH (POWER1)

Size

e	Document Number
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LLW-1 / LGG-1

Date	Time	Location	Activity	Remarks
10/10/2023	08:00	Lab 1	Introduction to the course	Students received an overview of the course structure and objectives.
10/10/2023	09:00	Lab 2	Basic circuit analysis	Students performed a series of experiments on basic circuit analysis.
10/10/2023	10:00	Lab 3	AC circuit analysis	Students performed a series of experiments on AC circuit analysis.
10/10/2023	11:00	Lab 4	Power in AC circuits	Students performed a series of experiments on power in AC circuits.
10/10/2023	12:00	Lab 5	Thévenin's theorem	Students performed a series of experiments on Thévenin's theorem.
10/10/2023	13:00	Lab 6	Superposition theorem	Students performed a series of experiments on the superposition theorem.
10/10/2023	14:00	Lab 7	Maximum power transfer	Students performed a series of experiments on maximum power transfer.
10/10/2023	15:00	Lab 8	Resonance in AC circuits	Students performed a series of experiments on resonance in AC circuits.
10/10/2023	16:00	Lab 9	Impedance matching	Students performed a series of experiments on impedance matching.
10/10/2023	17:00	Lab 10	Final project presentation	Students presented their final project results.

te: Tuesday, January 18, 2011

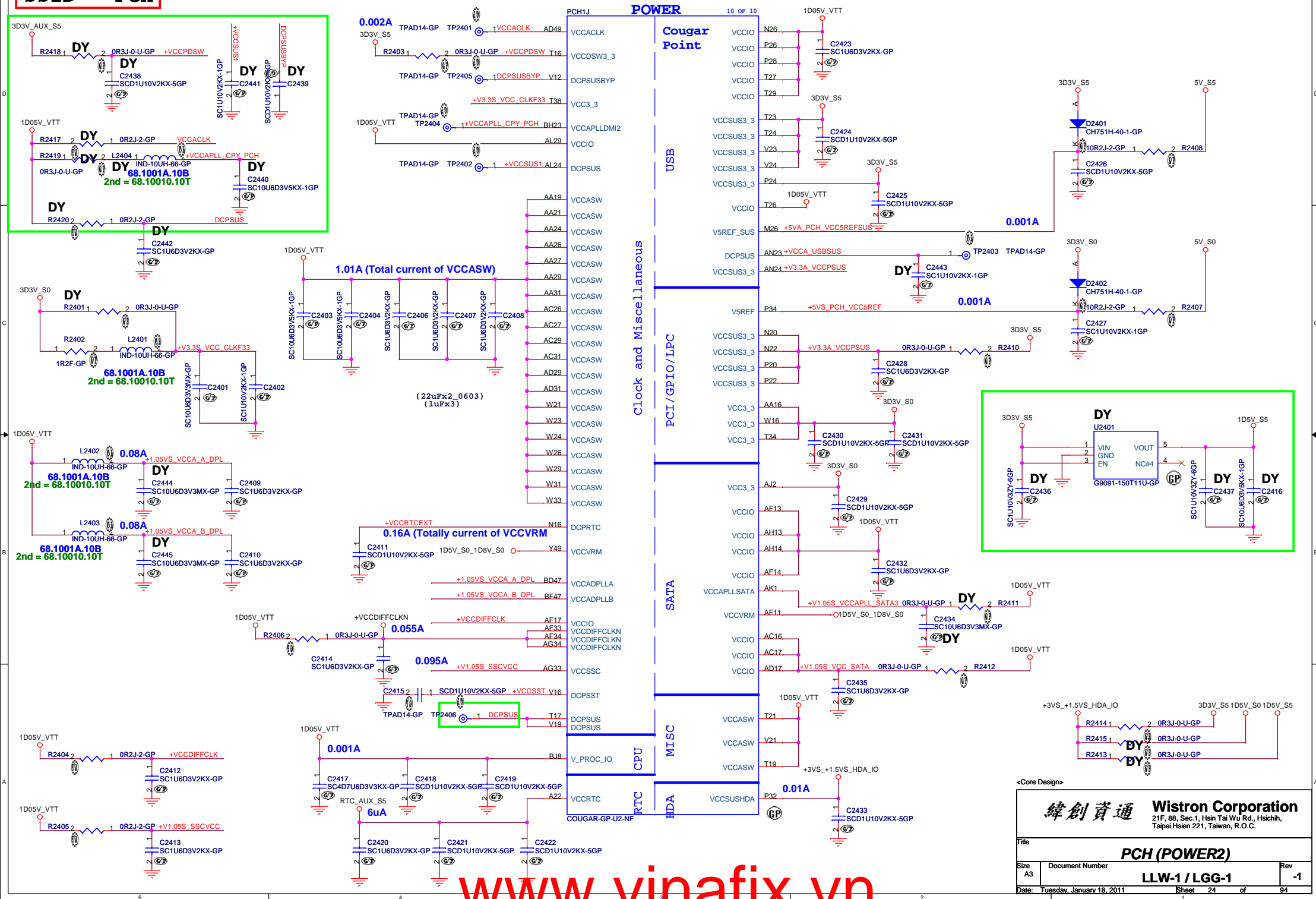
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Rev

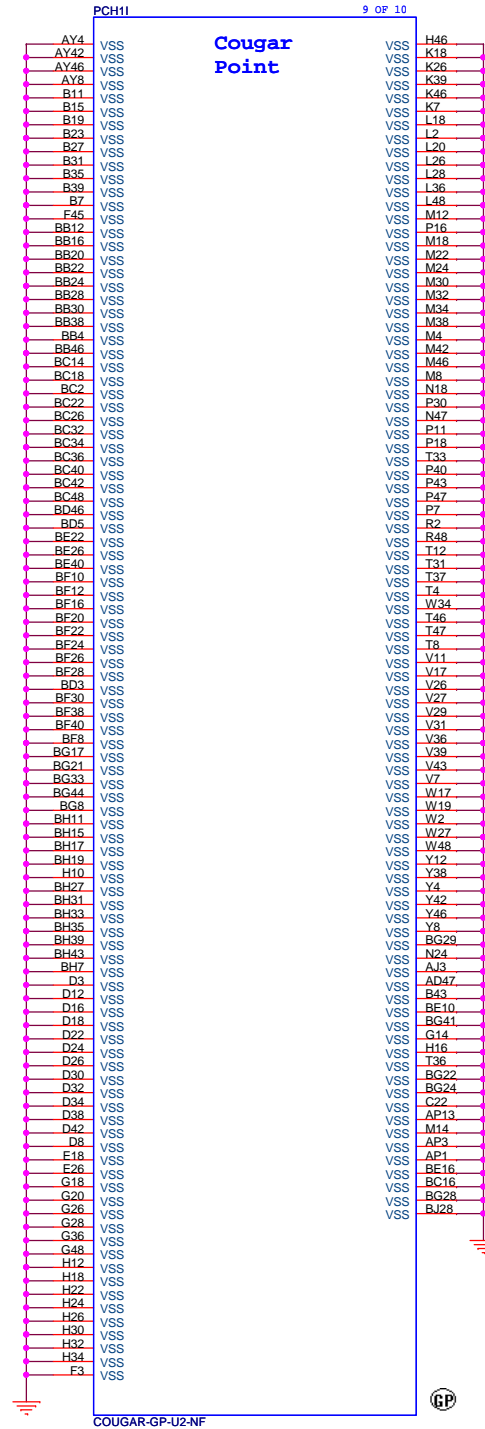
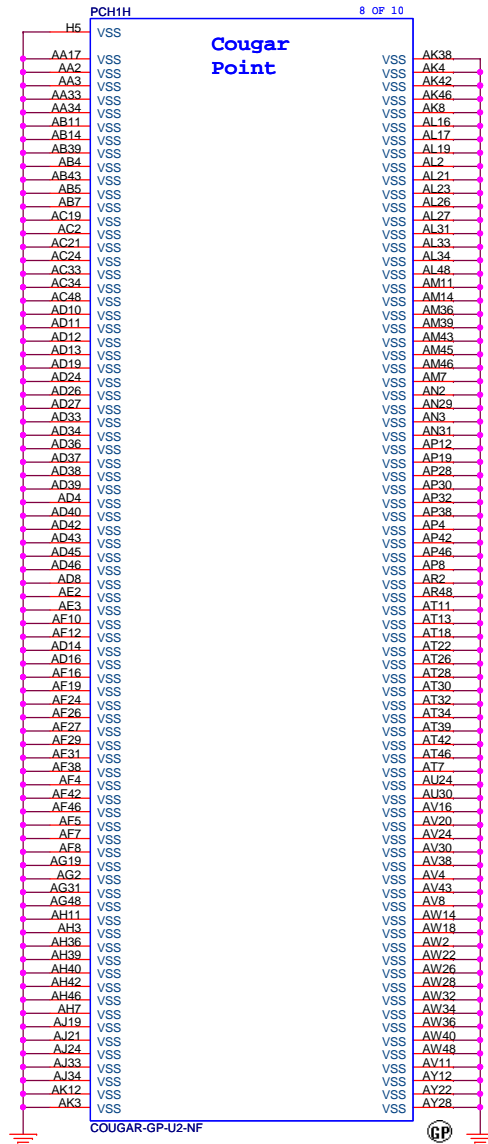
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94

SSID = PCH



SSID = PCH



BLANK

<Core Design>

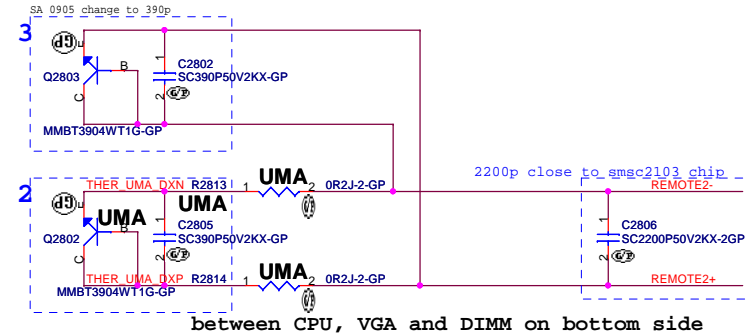
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	LLW-1 / LGG-1	-1
Date: Tuesday, January 18, 2011		Sheet 26 of 94



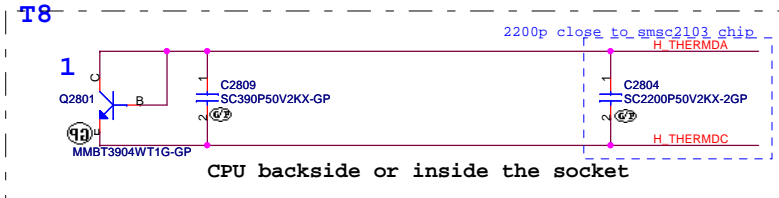
SSID = Thermal

Thermal sensor

Close to SO-DIMM side.



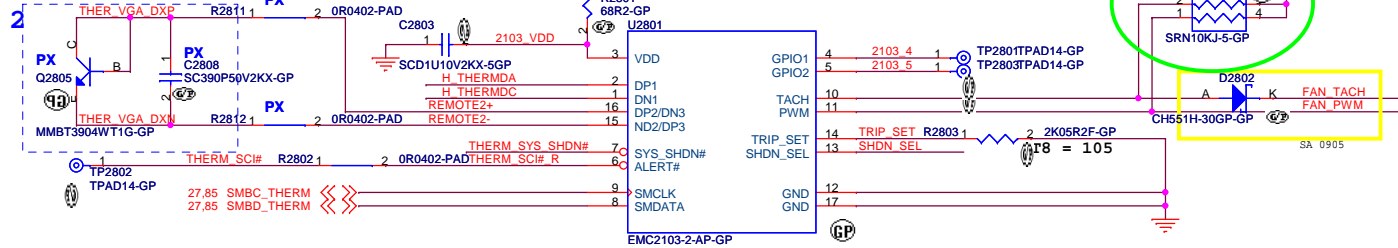
T8



CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

Close to VGA side.



pin6, ALERT# OD
pin7, SYS_SHDN# OD

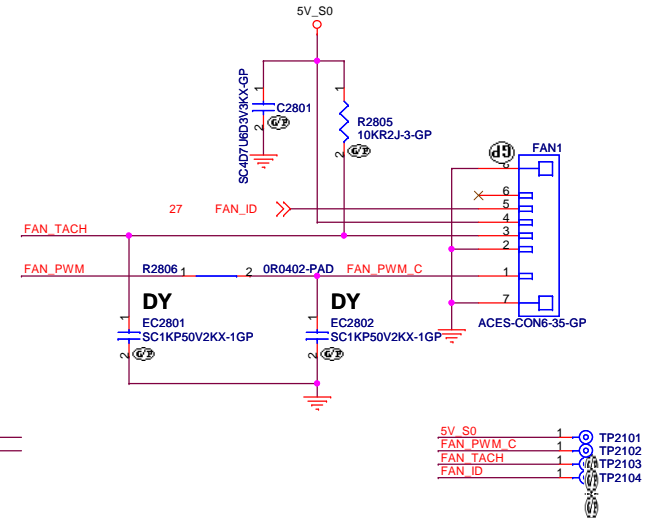
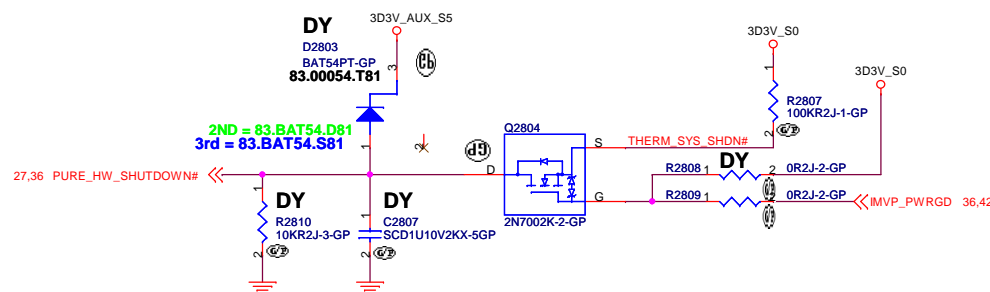


Table 28.1- General Purpose Transistors multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11
CHENMKO	CH3904WGP	N/A	84.03904.Y11

Table 28.2- Surface Mount Schottky Barrier

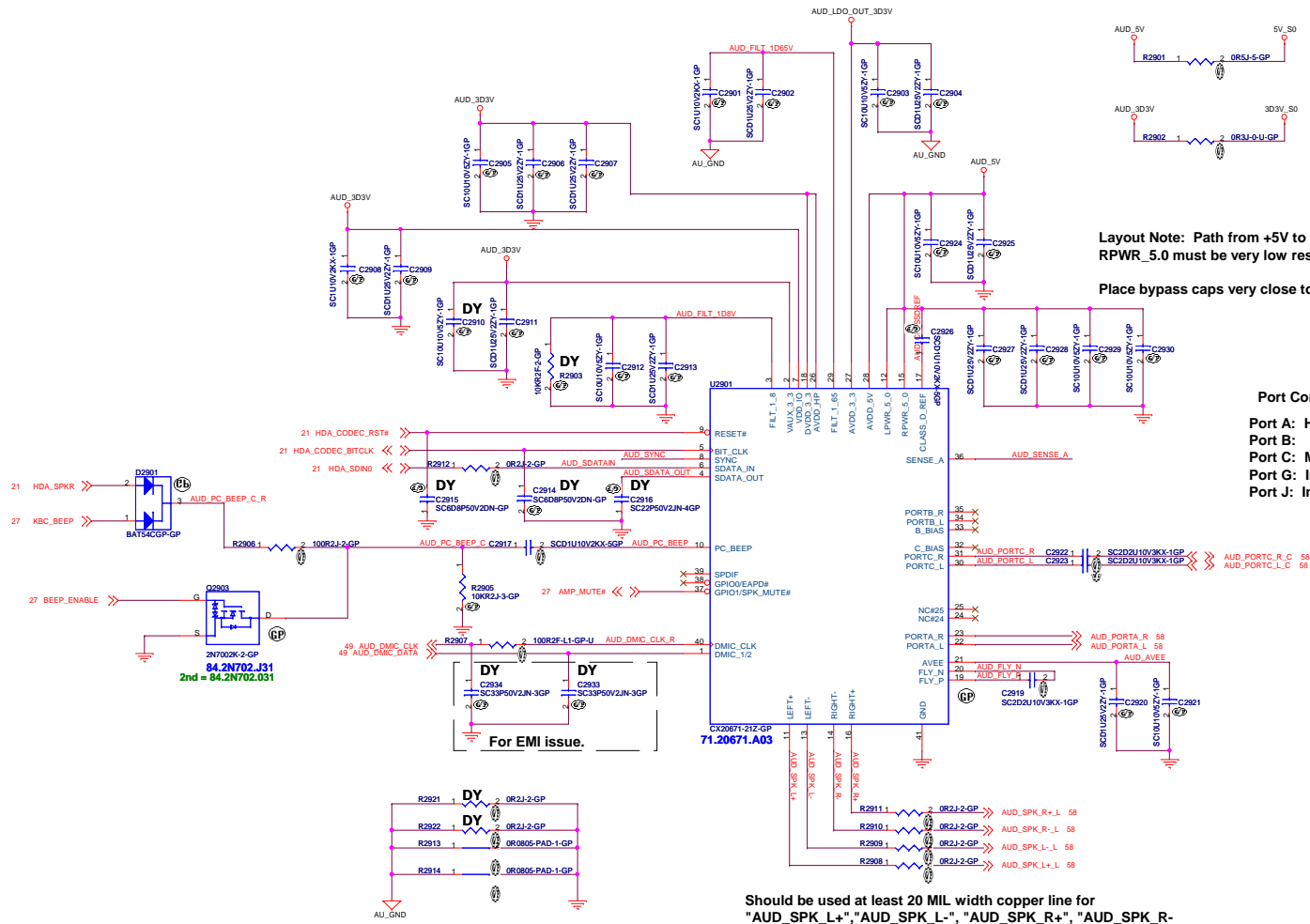
Supplier	Description	Lenovo P/N	Wistron P/N
CHENMKO	BAT54PT	N/A	83.00054.T81
PANJIT	BAT54	N/A	83.BAT54.D81
Power Silicon Inc.	BAT54C	N/A	83.BAT54.S81

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Title	Document Number	Rev
THERMAL SENSOR SMSC EMC2103	LLW-1 / LGG-1	-1
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AUDIO CODEC



Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

Port Configuration

Port A: Headphone jack

Port B:

Port C: Microphone jack

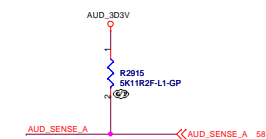
Port G: Internal stereo speakers

Port J: Internal stereo digital mic

JACK DETECT RESISTORS

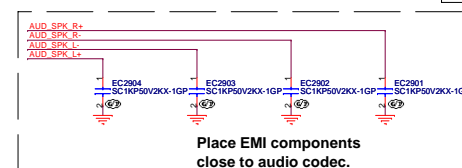
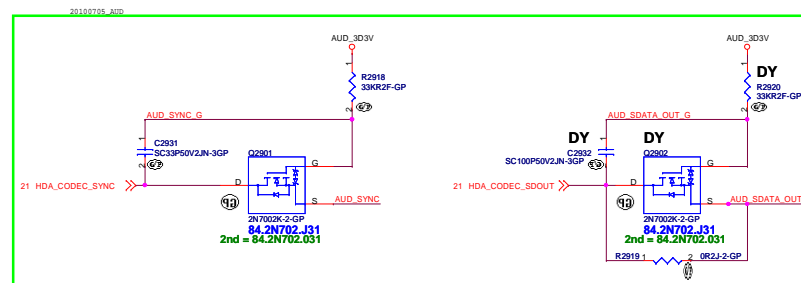
Close to Pin36

SENSE PIN A



Should be used at least 20 MIL width copper line for
"AUD_SPK L+", "AUD_SPK L-", "AUD_SPK R+", "AUD_SPK R-

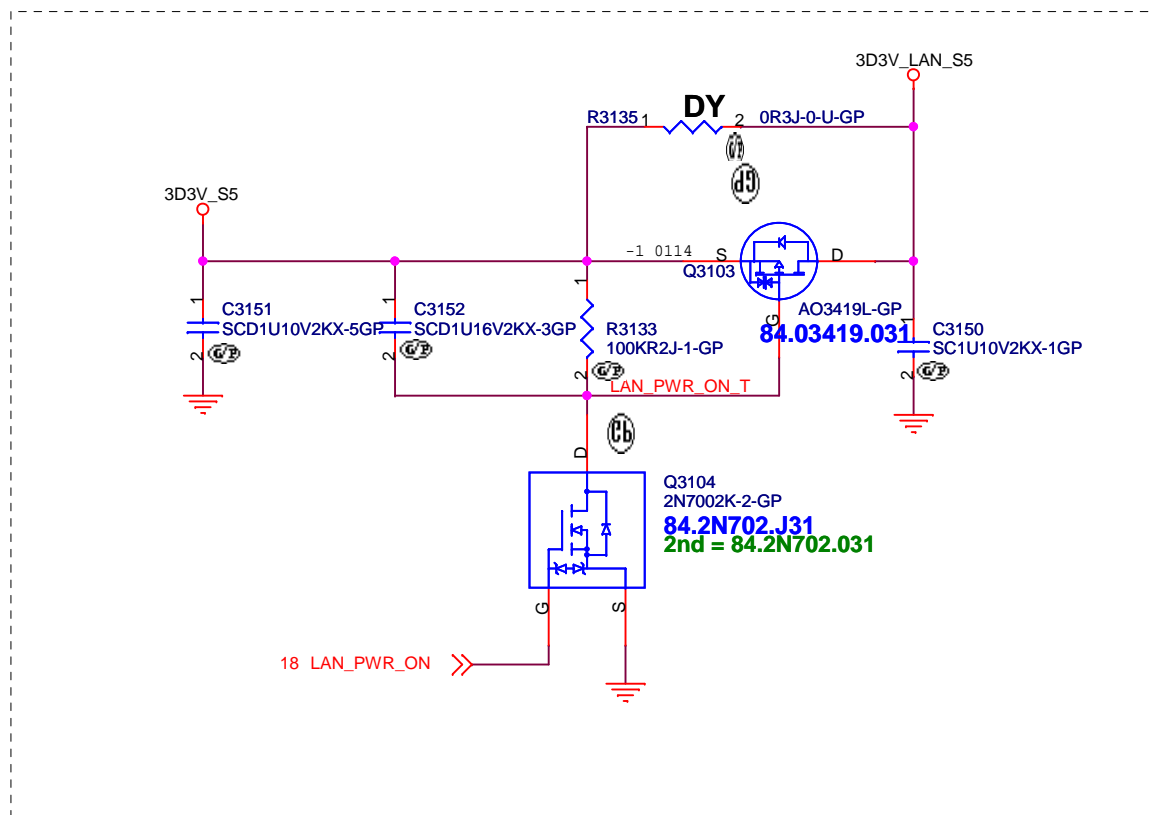
**Place R2913/R2914 under CODEC,
and place R2921/R2922 near CODEC**





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Title			
AMP			
Size	Document Number		Rev
A3	LLW-1 / LGG-1		-1
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Title

LAN PWR SW

Size

Document Number

Rev

LLW-1 / LGG-1

-1

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Please place these capacitors, for PCIE_VOUT as close to R5U220 as possible.

Please place these capacitors for VCC_3Vx as close to R5U220 as possible

Please apply wide trace for MF_VOUT between R5U220 and SD Card Slot.
- 2A (W=2mm) Recommended.
- Please consider the number of vias when layer of MF_VOUT is changed.

Please apply capacitors for MF_VOUT as close as possible to connector Otherwise

Please apply external parts, R456, C457, R415 for RXC, CPO, and RREF, as close as possible to R5U220.

Please place these capacitors, for PCIE_VIN as close to R5U220 as possible.

RICOH recommends strongly, Trace length Difference among these SDXC signals are smaller than 0.5 inches.
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

RICOH recommends strongly, the trace length for these SDXC signals are less than 6-inches.
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

Please apply capacitor C3210 for SD18C as close as possible to R5U220.

Please apply 50 ohm impedance control for these SDXC signals:
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

Please use Microstrip trace routing for these SDXC signals
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

MEDIA I/F	SD/MMC	MEMORYSTICK	XD
MFIO00	SDWP#	MSBS	XD_D7
MFIO01	SD_D1		XD_D6
MFIO02	SD_D0	MS_D1	XD_D5
MFIO03	(SD_D7)		XD_D4
MFIO04	(SD_D6)	(MS_D5)	XD_D3
MFIO05	SD_CLK	MSD0	XD_D2
MFIO06			XD_D1
MFIO07	(SD_D5)	(MS_D4)	XD_D0
MFIO08	SD_CDM	MS_D2	XD_WP#
MFIO09	(SD_D4)	(MS_D6)	XD_WE#
MFIO10	SD_D3	MS_D3	XD_ALE
MFIO11	SD_D2		XD_CLE
MFIO12			XD_CE#
MFIO13		(MS_D7)	XD_RE#
MFIO14		MS_CLK	XD_R/B
MFCD0#	SDDC#		XDCD0#
MFCD1#		MSINS#	XDCD1#

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Title R5U220 (CARD READER)

Size A3 Document Number LLW-1 / LGG-1 Rev -1

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<div>Title1394</div>		
<div>SizeA4</div>	<div>Document NumberLLW-1 / LGG-1</div>	<div>Rev-1</div>
<div>Date: Tuesday, January 18, 2011</div>		<div>Sheet 33 of 94</div>

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Title <div>Smart Card Reader</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
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Title

USB3.0

Size

A4

Document Number

LLW-1 / LGG-1

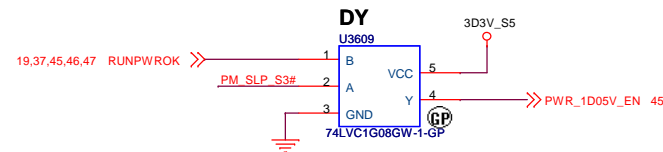
Rev

-1

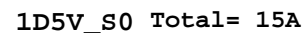
Date: Tuesday, January 18, 2011

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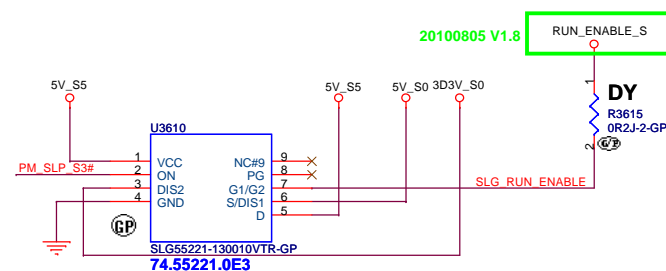
Power Sequence



Run Power



MAX Current 3000 mA
Design Current 2100 mA



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Title

POWER SEQUENCE

Size
A

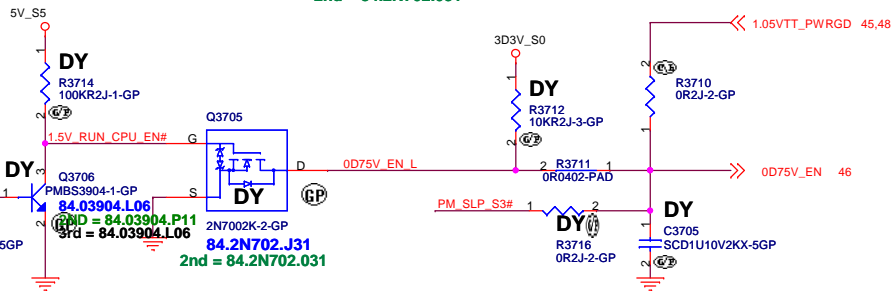
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LLW-1 / LGG-1

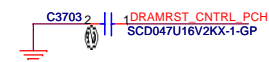
Date: Tuesday, January 18, 2011

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Rev	-1
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[illegible]

SM_DRAMPWROK must have a maximum of 15ns rise or fall time over $VDDQ \pm 0.55 \pm 200\text{mV}$ and the edge must be monotonic

[illegible]

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Title			
ADAPTER OCP / S3 reduction			
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Title <div>DCIN_JACK</div>		
Size	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
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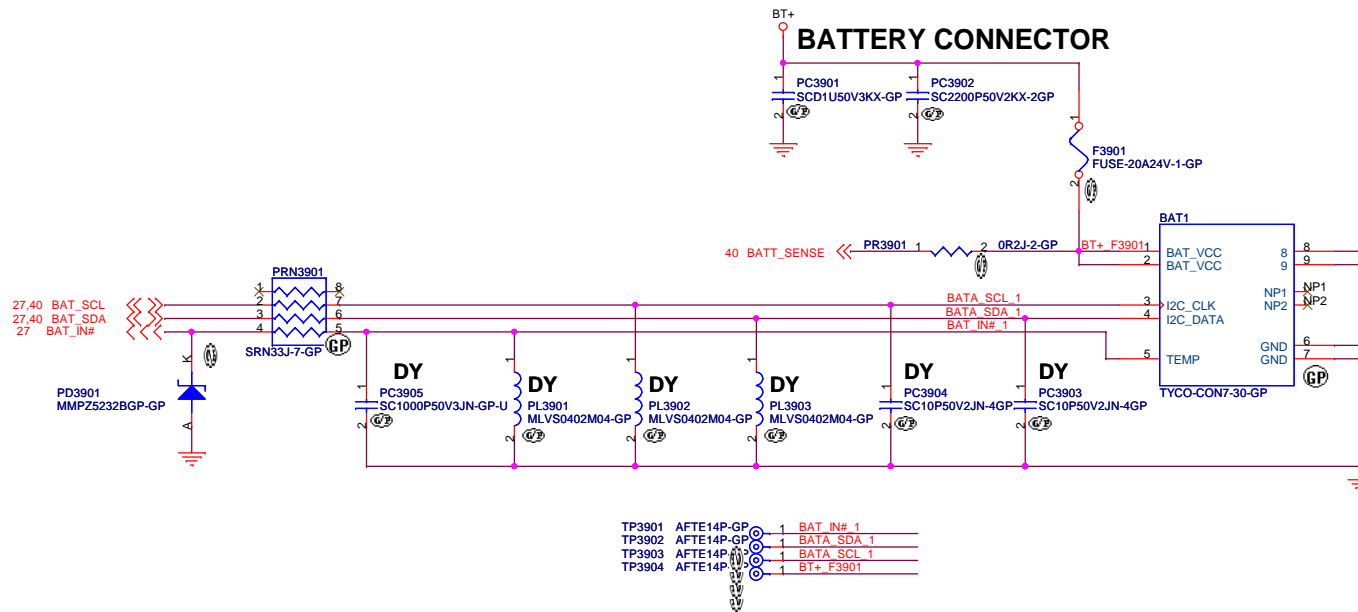


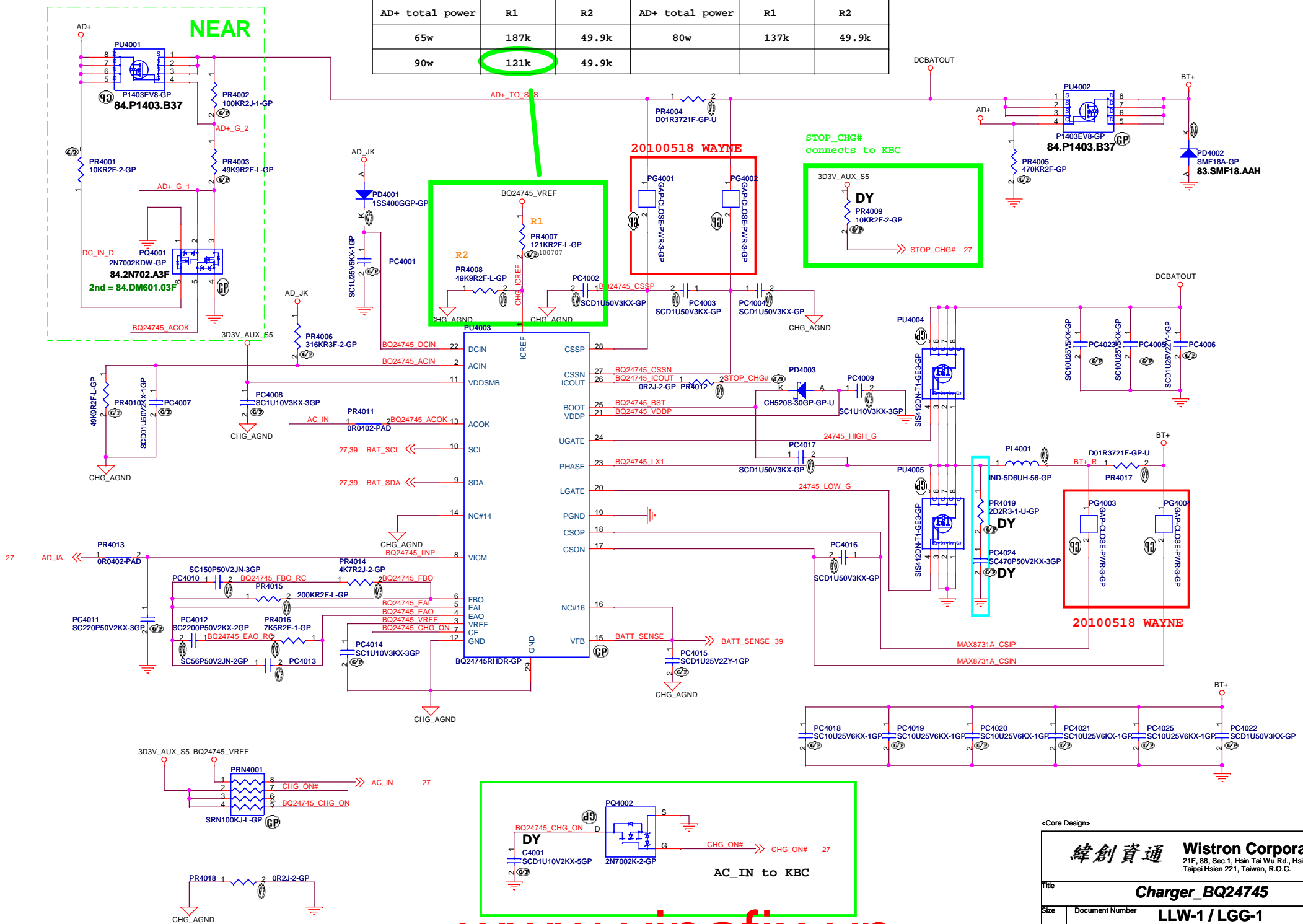
Table 39.1- Surface Mount Zener ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
CHENMKO	MMPZ5232BGP	N/A	83.5R603.R3F
DIODES	MMSZ5232BS-7-F	N/A	83.5R603.K3F
PANJIT	MMSZ5232BS	N/A	83.5R603.Q3F

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Title BATT_CONN	
Size Document Number LLW-1 / LGG-1	Rev -1
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AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			



```
SSID = PWR.Plane.Regulator_5v3p3v
```

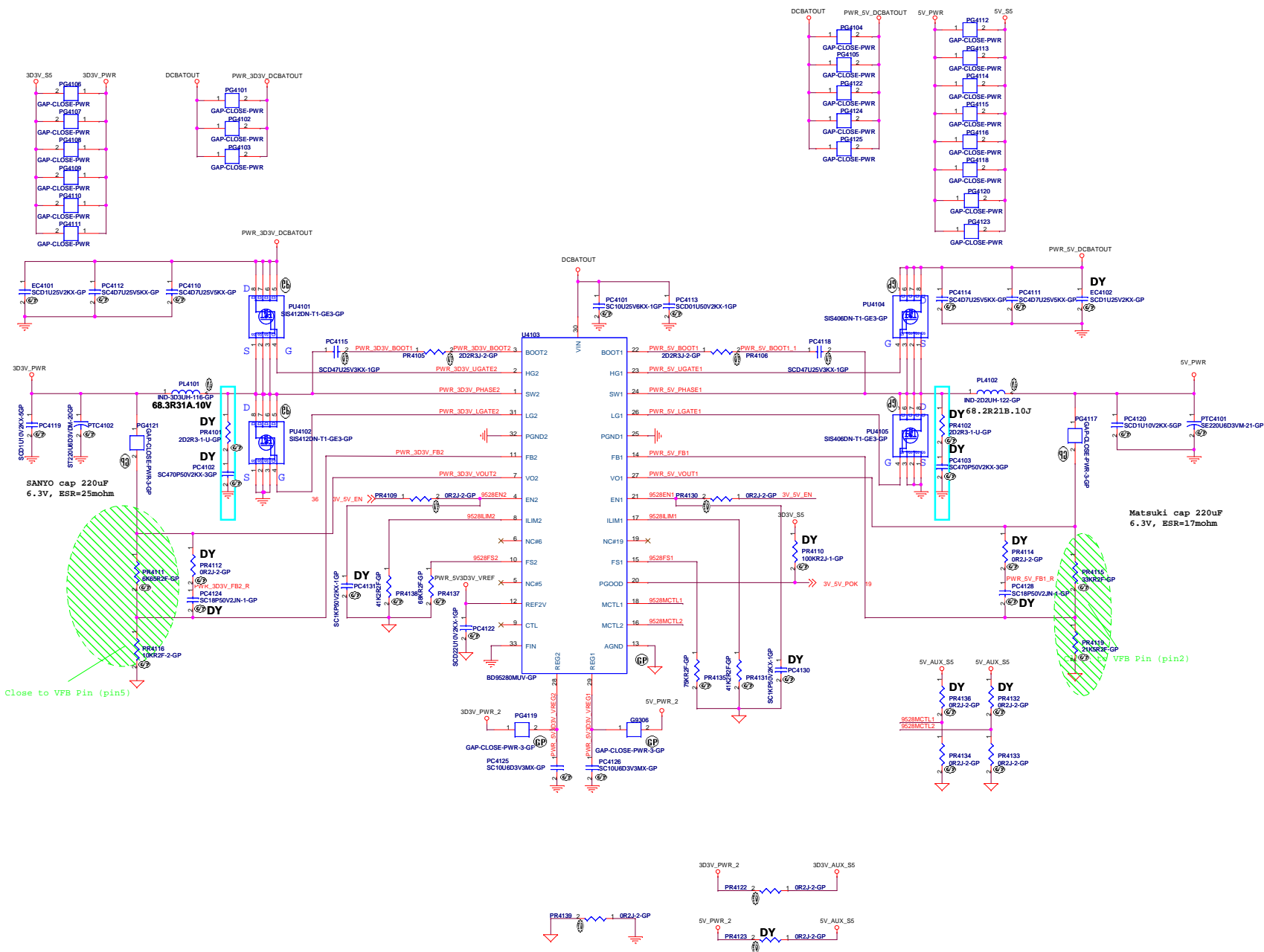


Table 41.1 - POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
SANYO	6TPE220MAP	N/A	77.22271.27L
NEC-TOKIN	V0J227M(25)12RE	N/A	77.C2271.00L

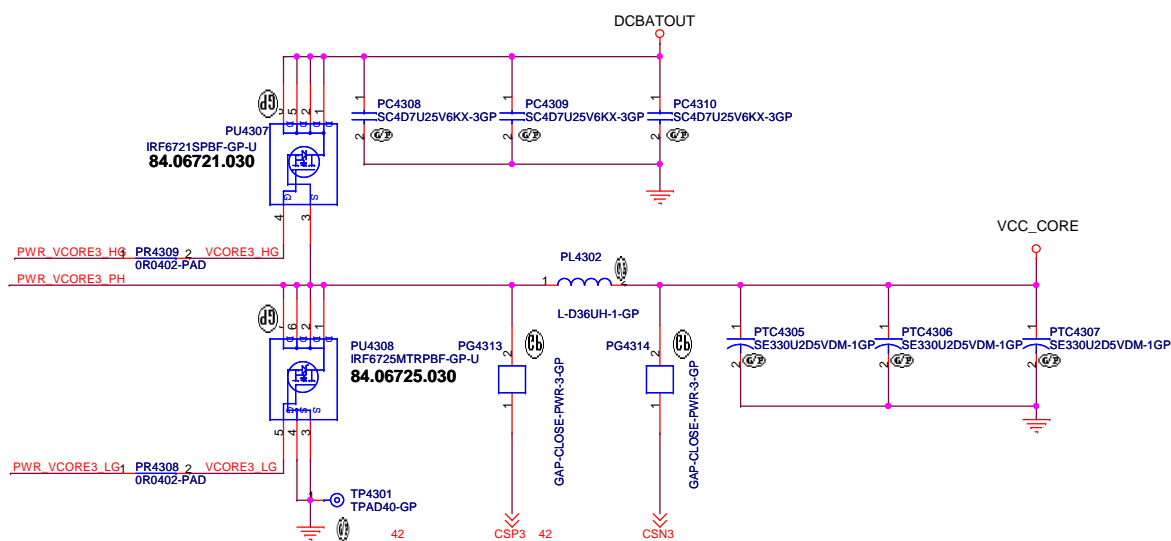
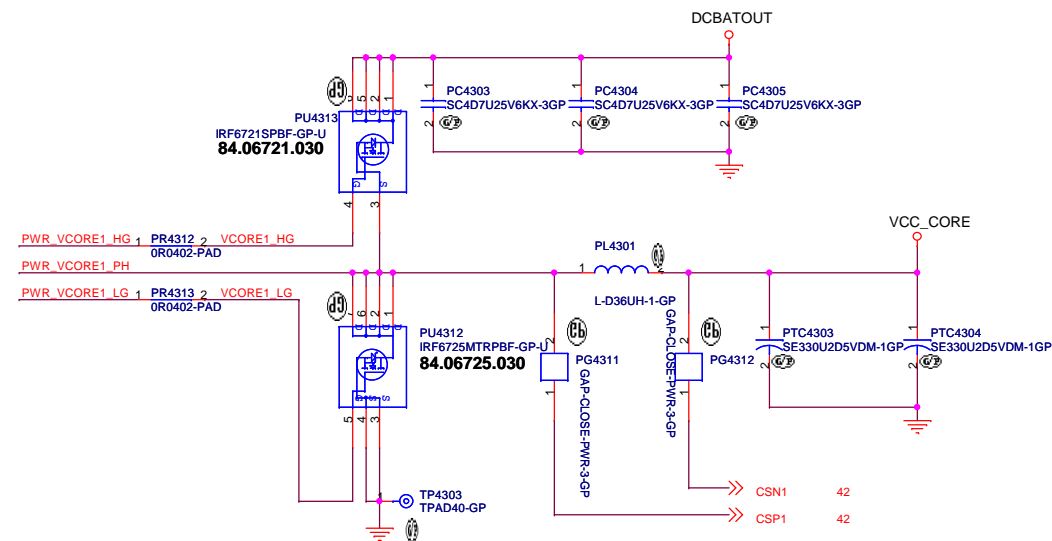
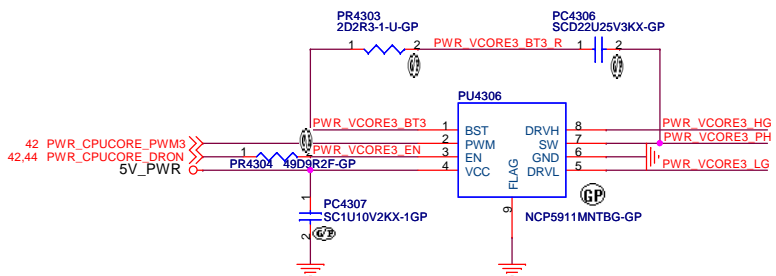
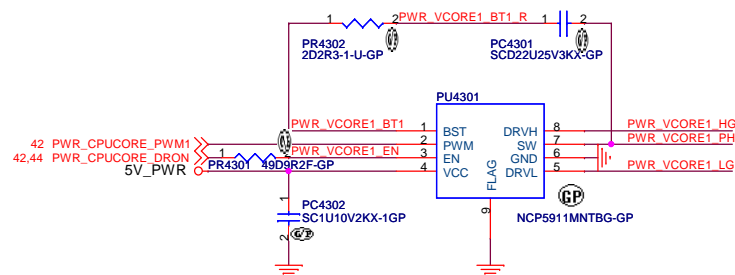
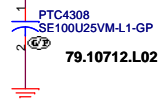
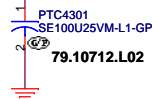
◀Core Design▶

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Title			
DC/DC 3D3V5V			
Size	Document Number		Rev
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DCBATOUT

DCBATOUT

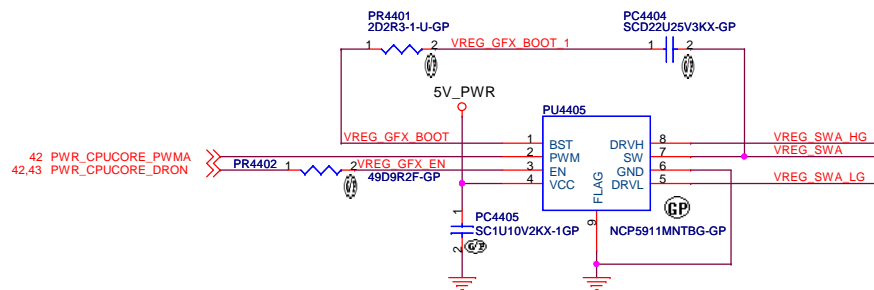
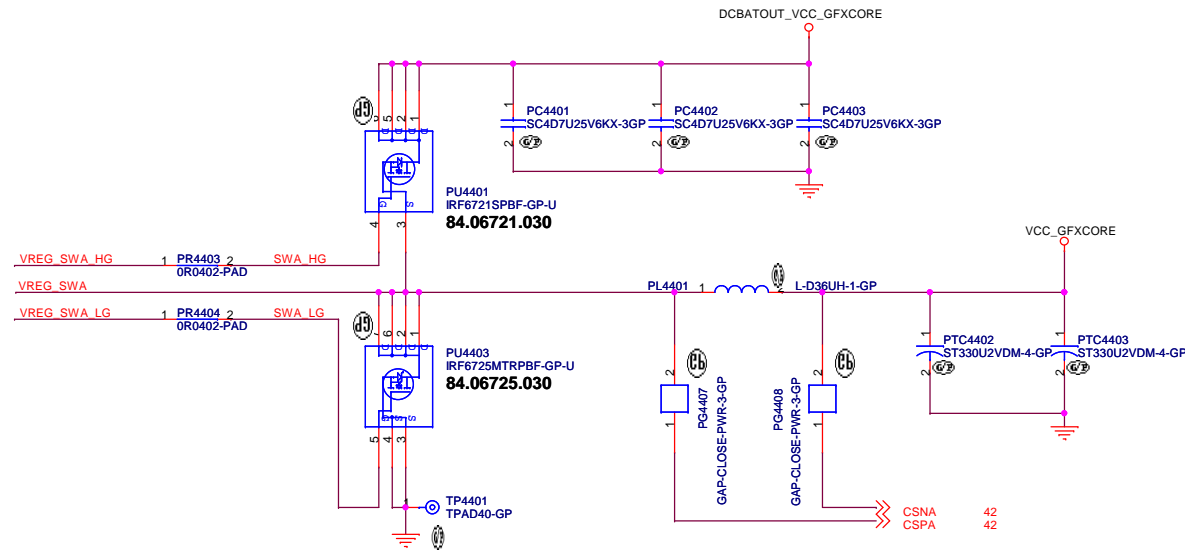
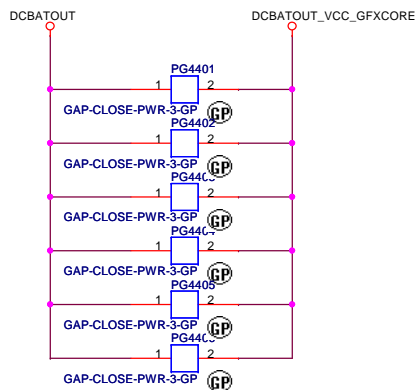


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Title **DC/DC CPU CORE2_NCP6131**
Size Document Number **LLW-1 / LGG-1** Rev **-1**

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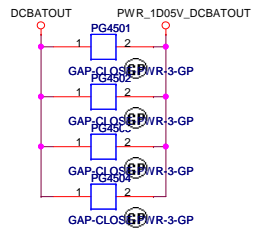


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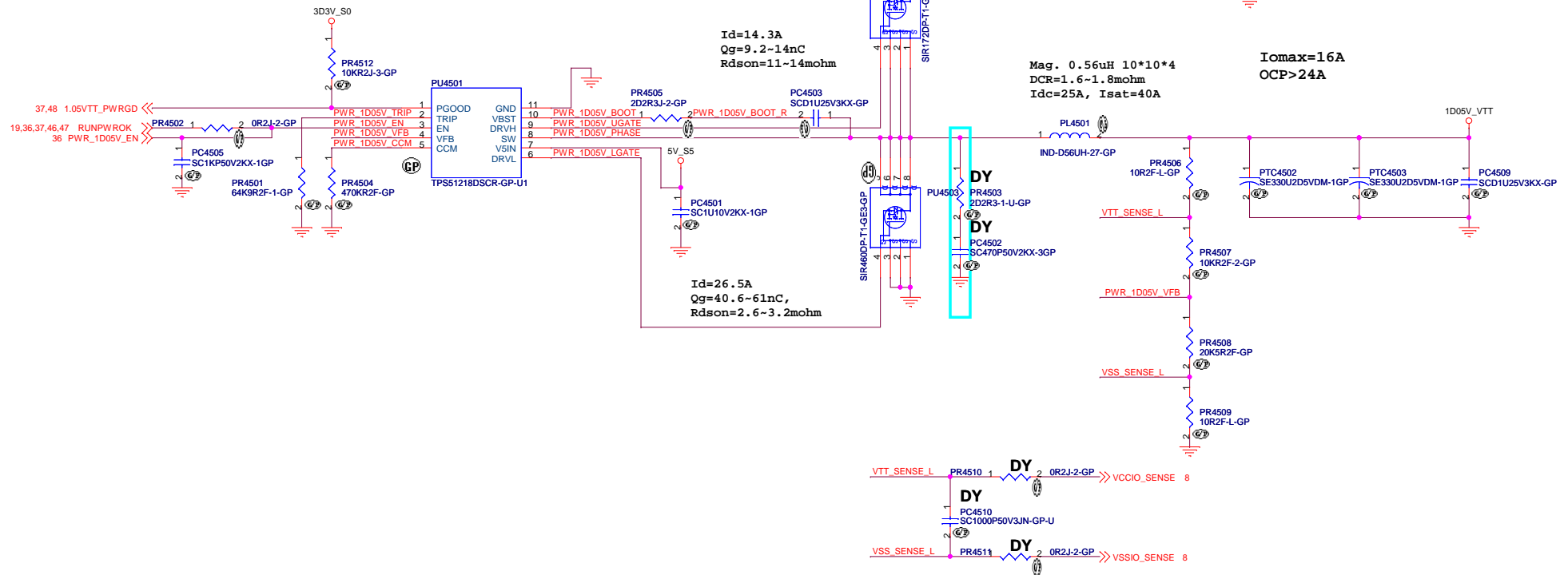
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Title			DC/DC CPU CORE3_NCP6131
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TPS51218 for 1D05V

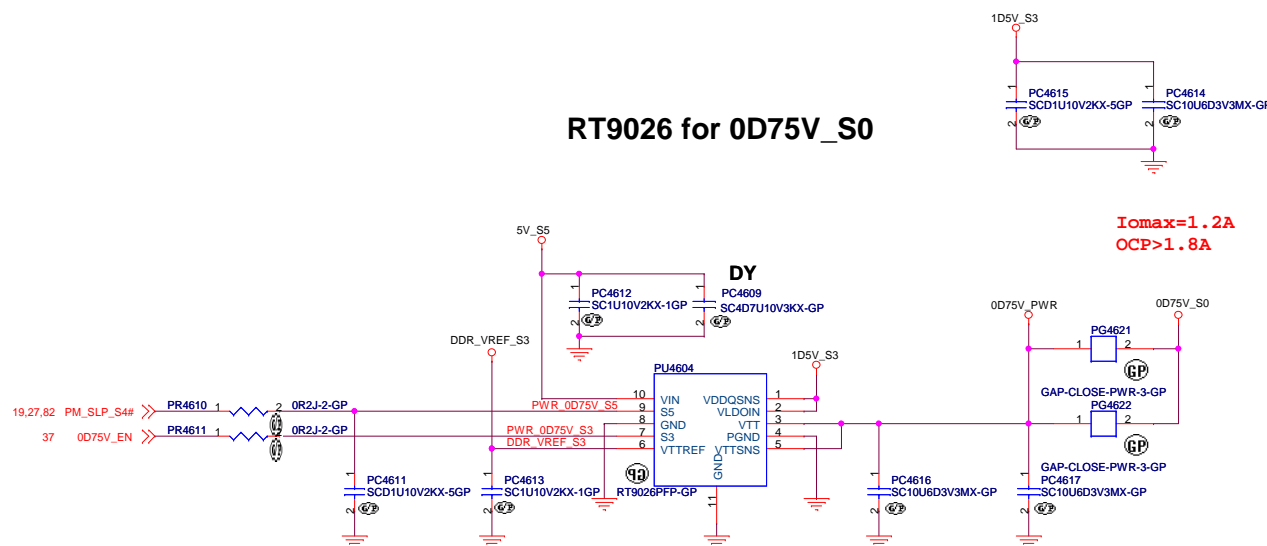
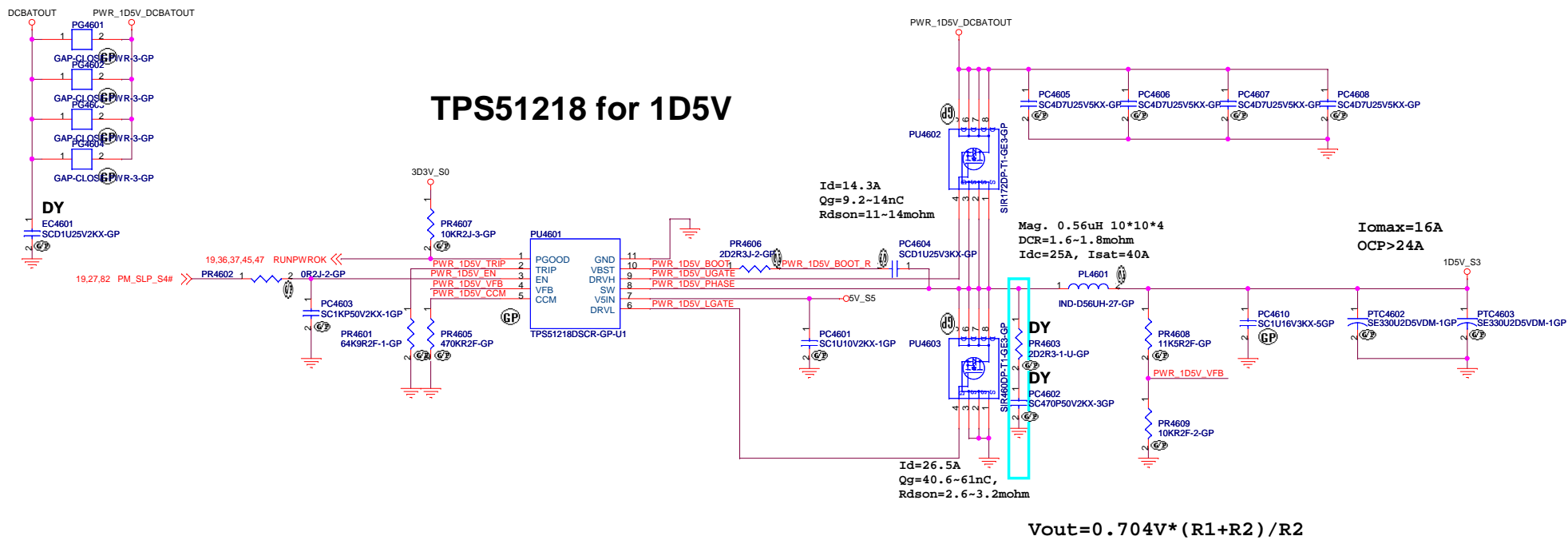


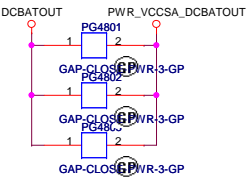
$$V_{out} = 0.704V \cdot (R1 + R2) / R2$$

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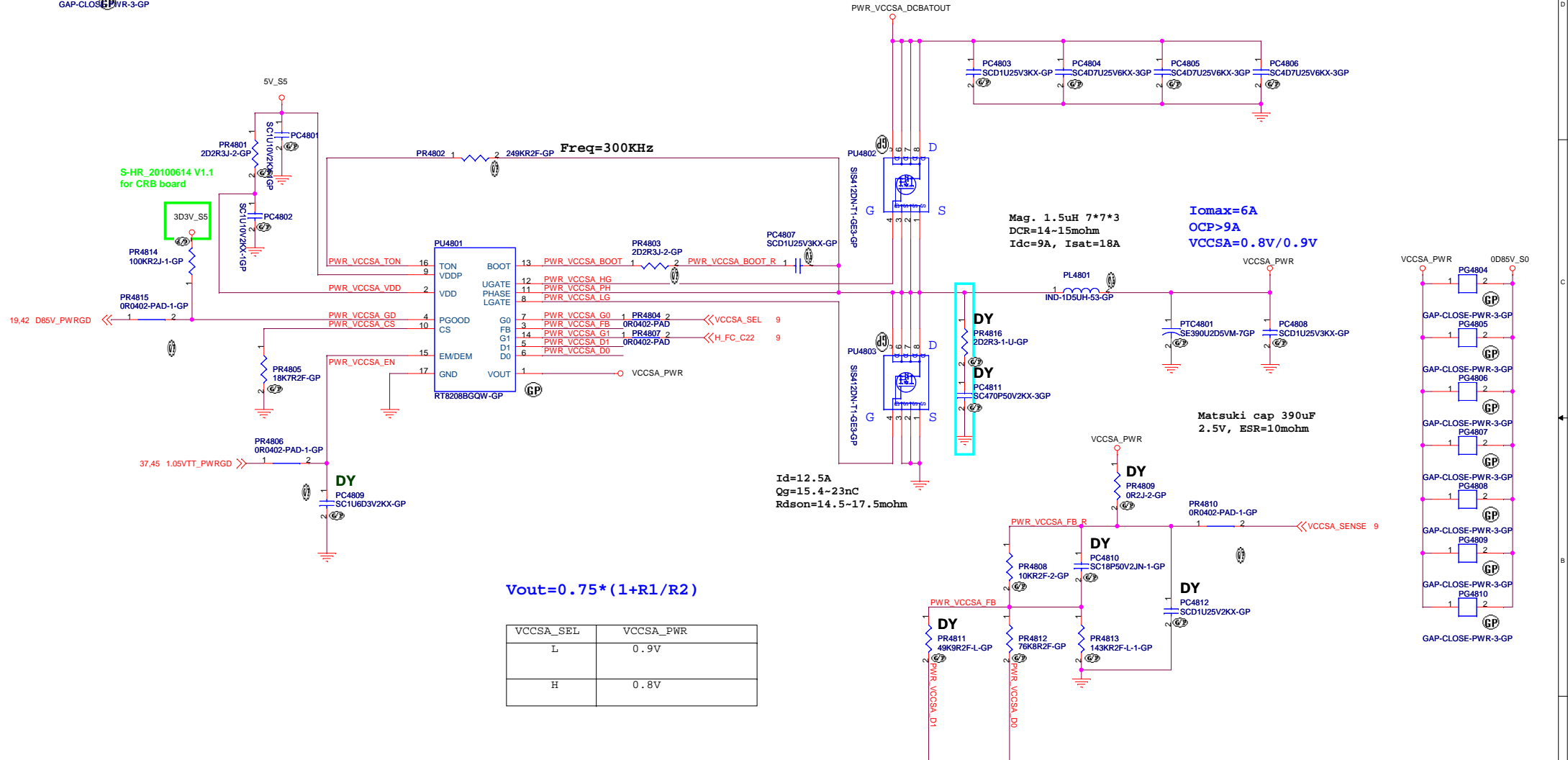
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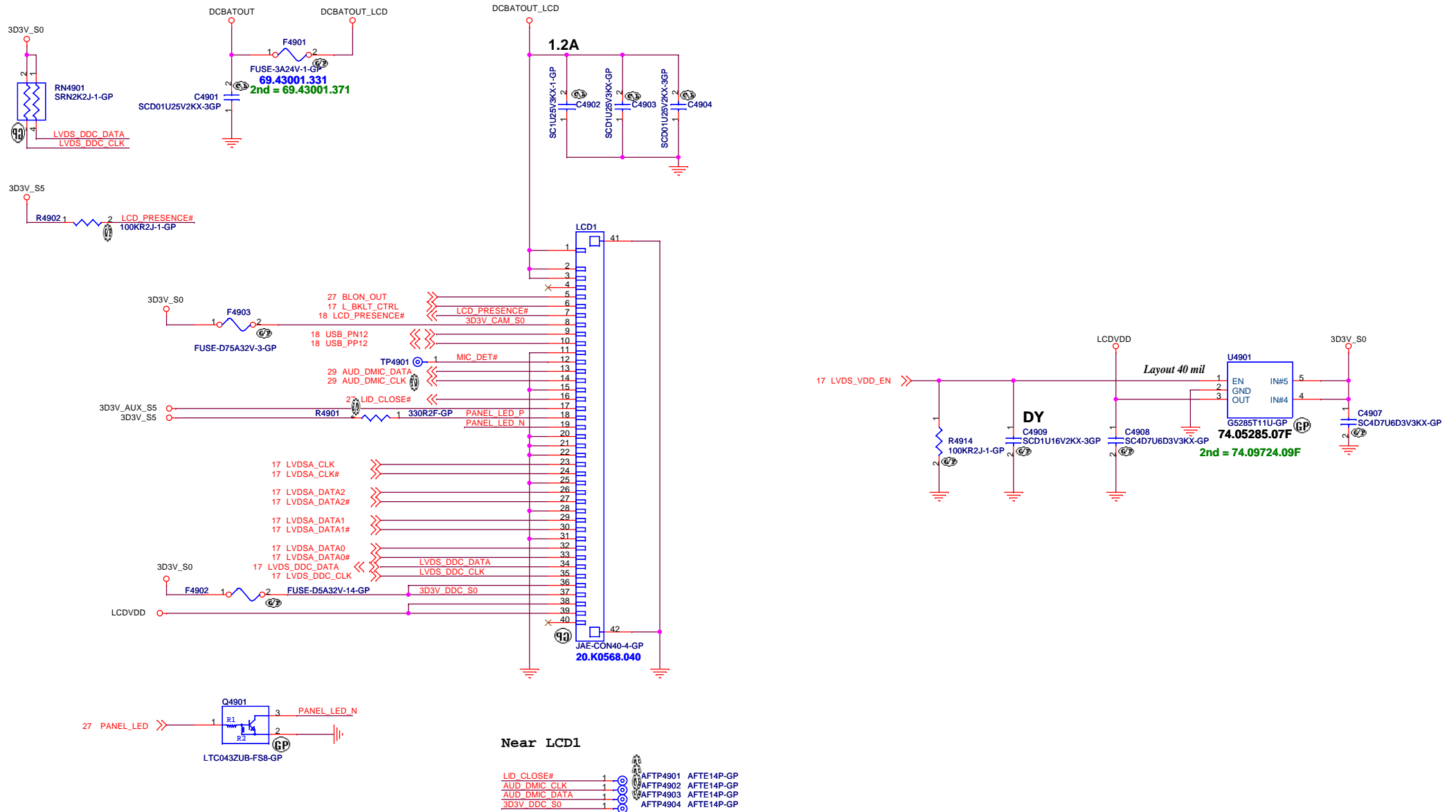
RT8208A for VCCSA



$$V_{out} = 0.75 * (1 + R1/R2)$$

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

LCD / Inverter Connector

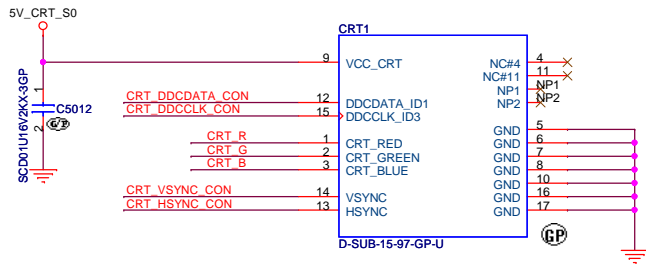


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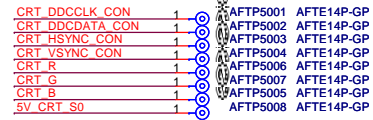
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LCD CONNECTOR		
Size A3	Document Number LLW-1 / LGG-1	Rev -1
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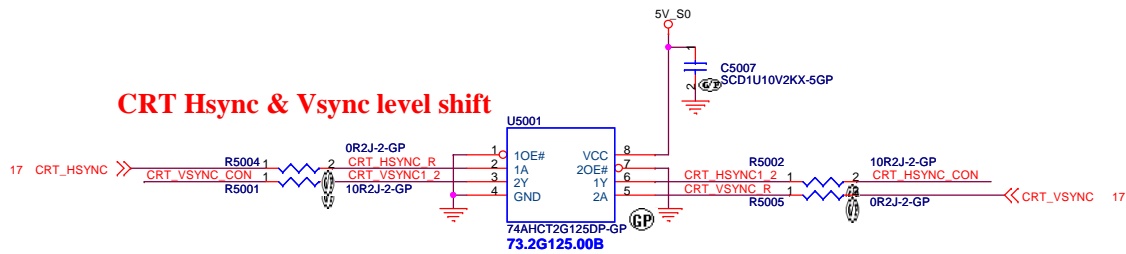
CRT CONNECTOR



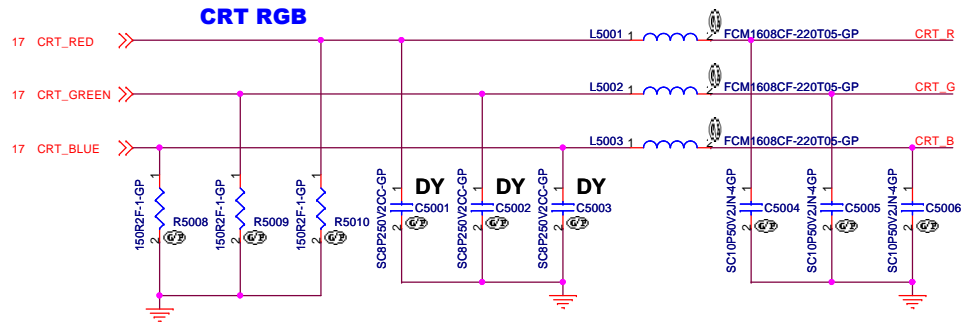
Near CRT1



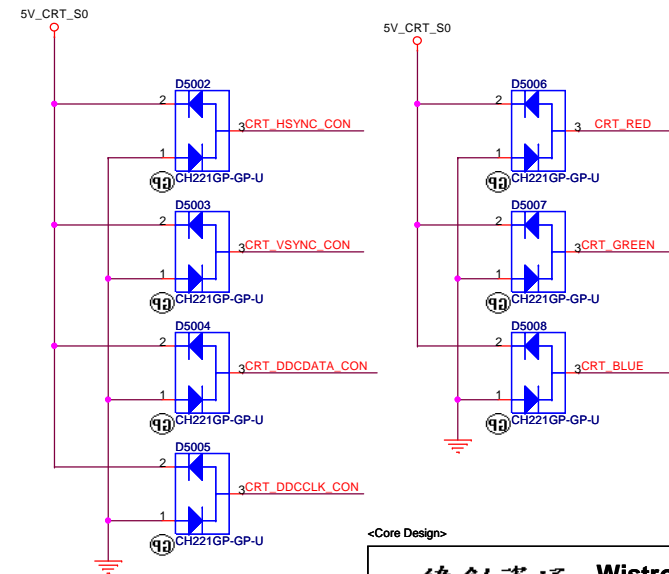
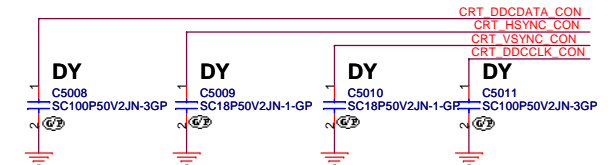
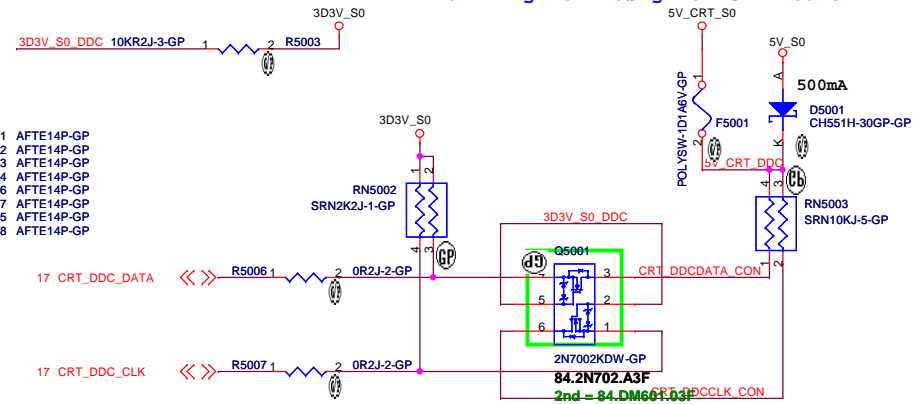
CRT Hsync & Vsync level shift

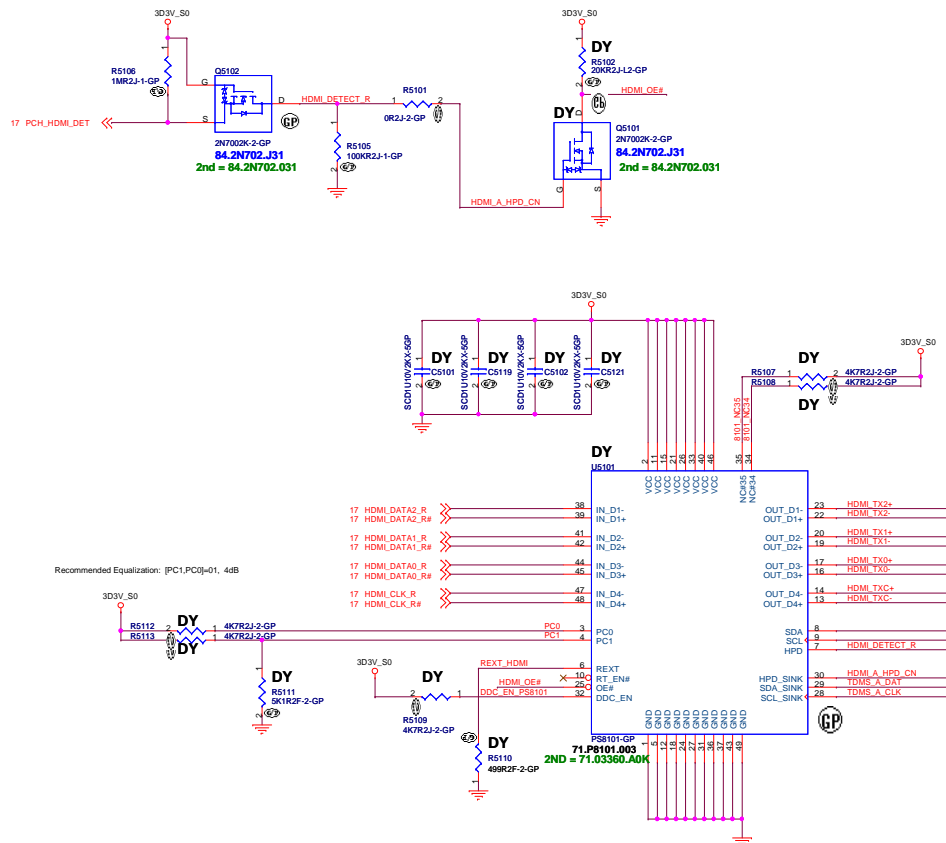


CRT RGB



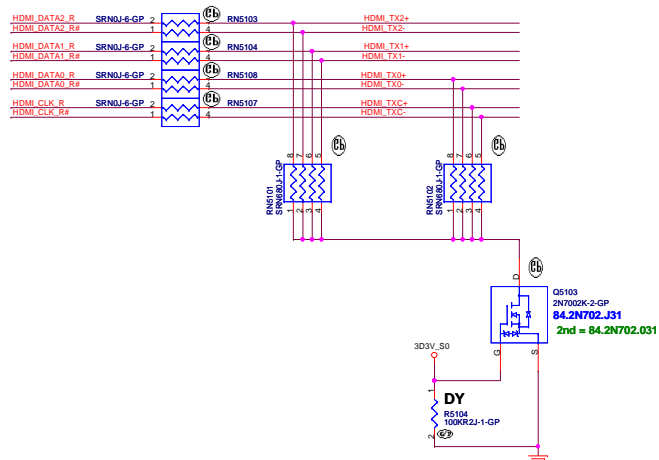
CRT DDCDATA & DDCCLK level shift



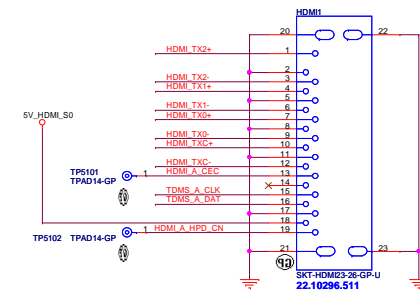
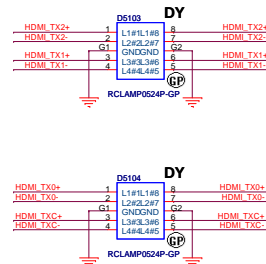


HDMI Passive Level Shifter

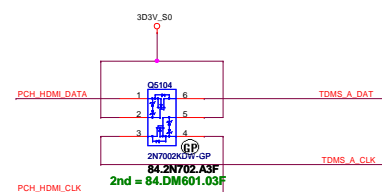
Close to HDMI Connector



HDMI Connector



HDMI DDC Passive Level Shifter



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Title **DISPLAY PORT CONNECTOR**

Size A4	Document Number LLW-1 / LGG-1	Rev -1
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D

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B

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Title		
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Size	Document Number	Rev
A4	LLW-1 / LGG-1	-1
Date: Tuesday, January 18, 2011		
Sheet 53 of 94		

D

C

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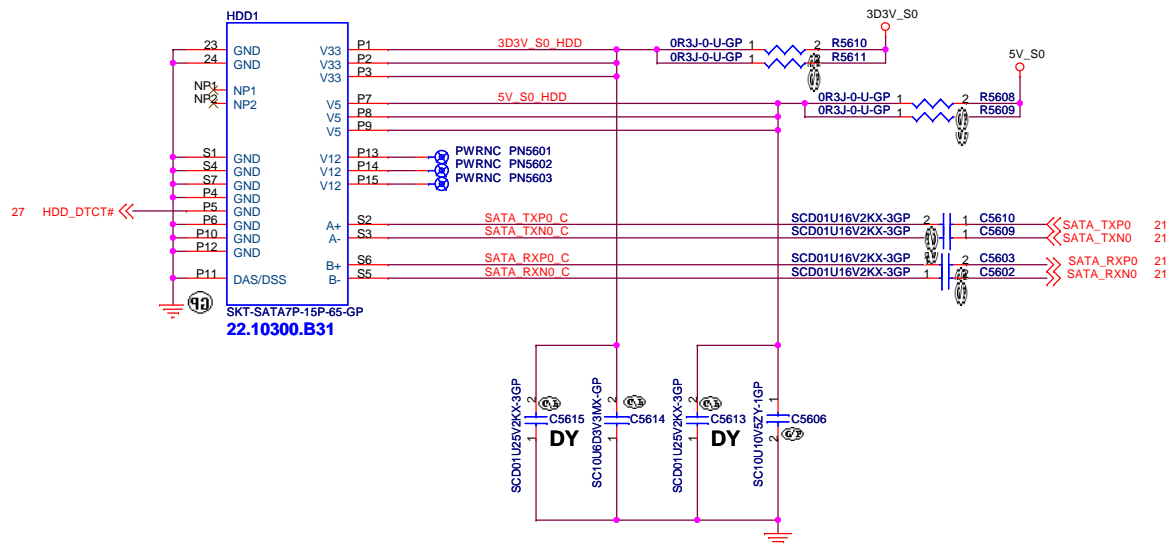
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Size A4	Document Number LLW-1 / LGG-1		Rev -1
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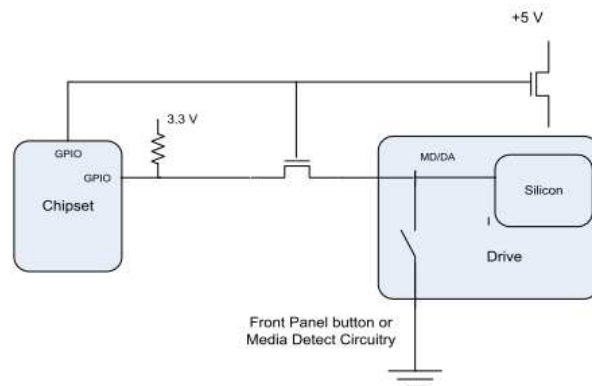
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Title <div>FAN CONTROL</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
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HDD Connector

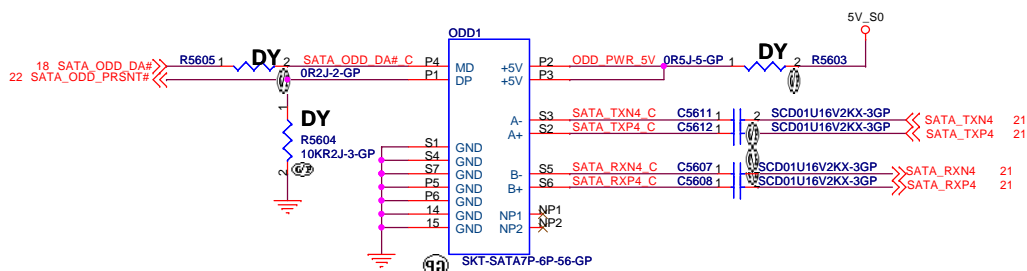


ODD Connector

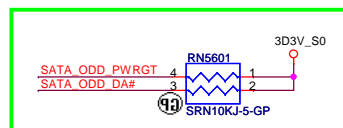
SATA_RX- and SATA_RX+ Trace Length match within 20 mil
Mars:
Exchange ODD and ESATA differential pair each other.



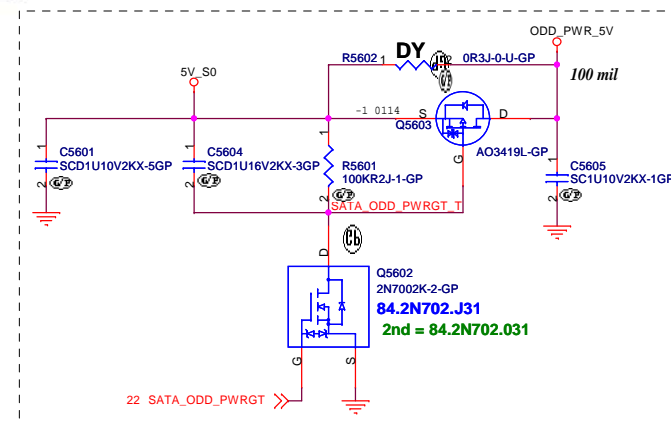
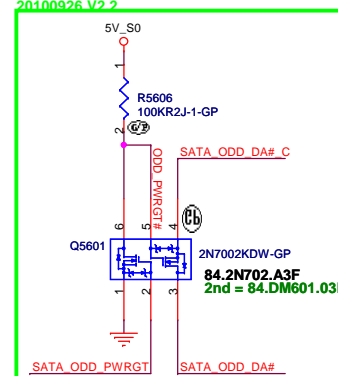
SATA Zero Power ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



SUPPORT ZERO SATA ODD



<Core Design>

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SATA HDD		
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ESATA Connector

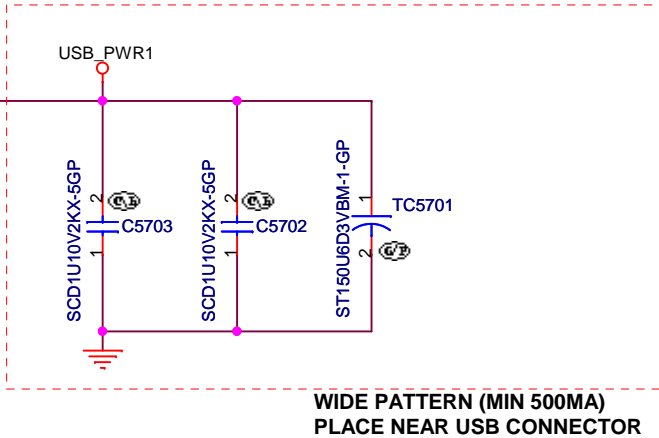
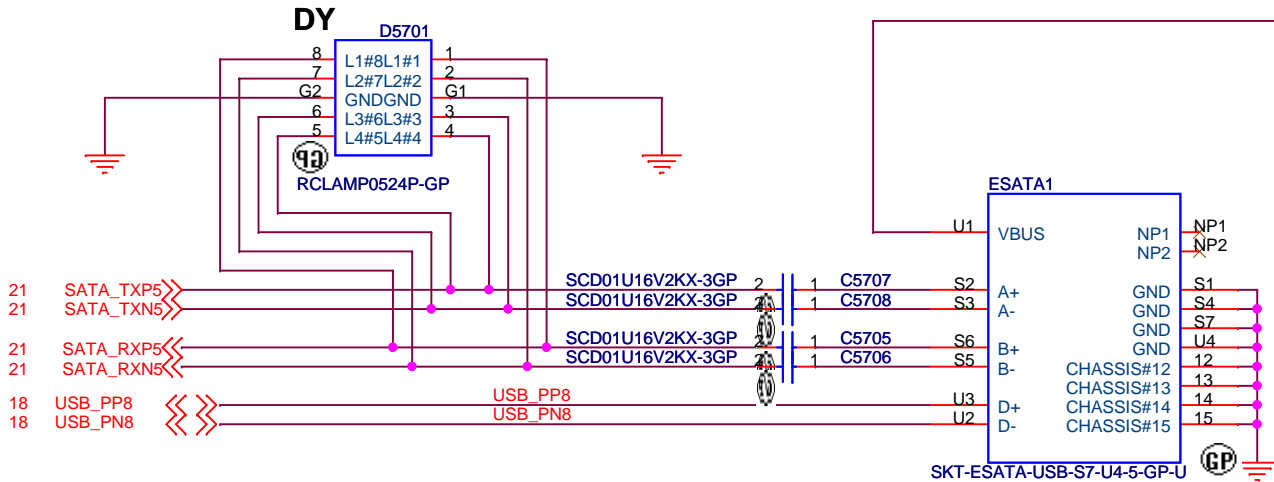
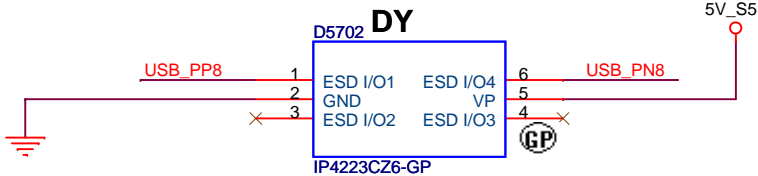
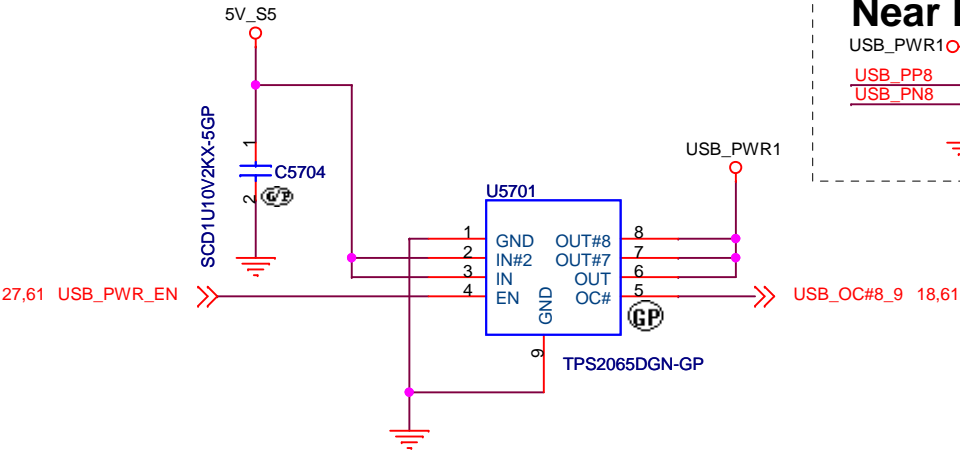
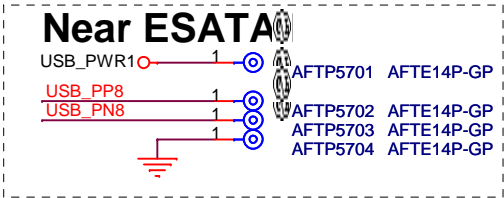


Table 57.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2065DGN4	54Y9024BA	74.02065.079
ROHM	BD8012FVJ	54Y9024AA	74.08012.07G

Table 57.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L



<Core Design>

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Title

ESATA CONNECTOR

Size A4

Document Number

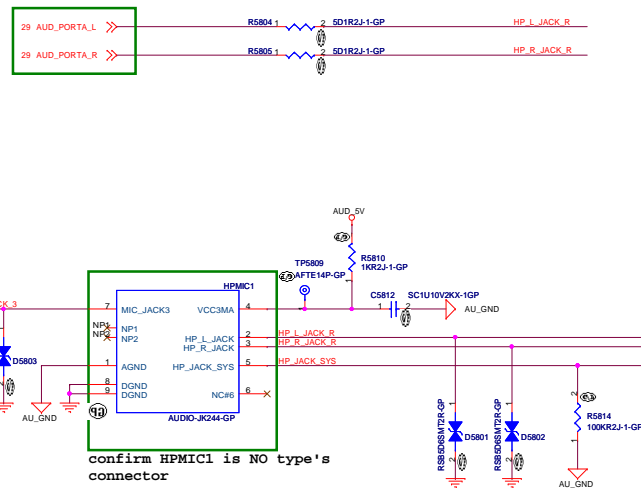
Rev -1

LLW-1 / LGG-1

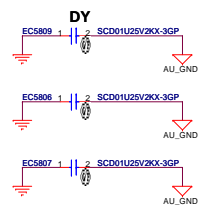
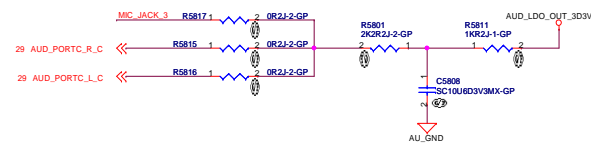
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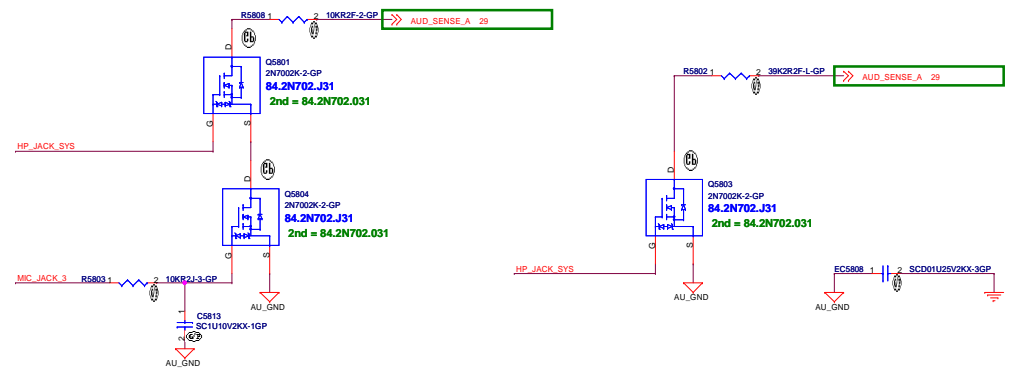
NEAR HEADPHONE CONN



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confirm HPMIC1 is NO type's
connector
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JACK SENSE



INTERNAL STEREO SPEAKERS

Port G

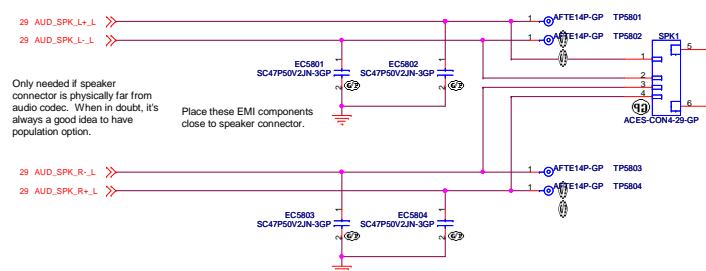

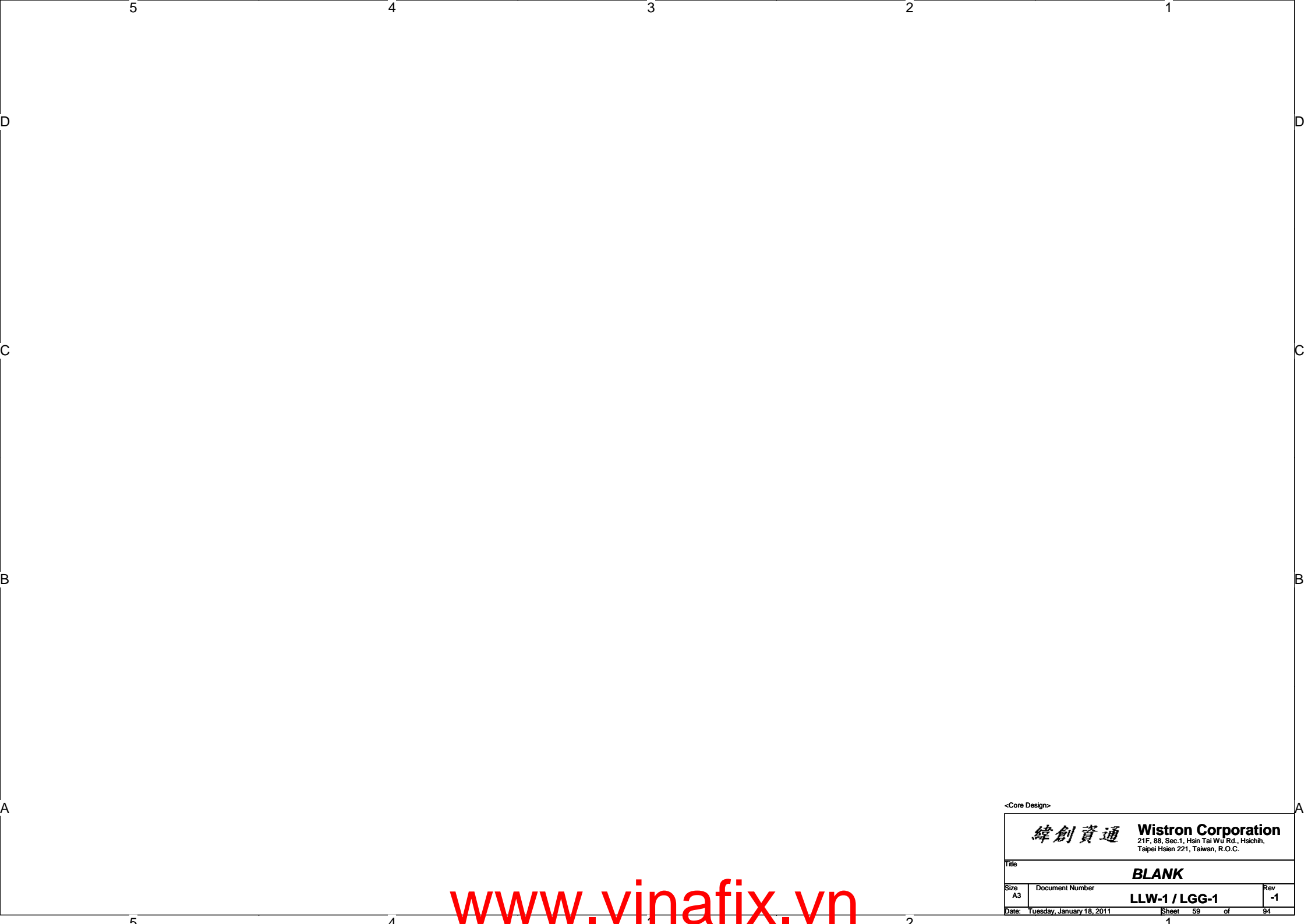


Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.B
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0
NXP	PESD5V0S1BB	N/A	83.0005V.0A

◀Core Design:

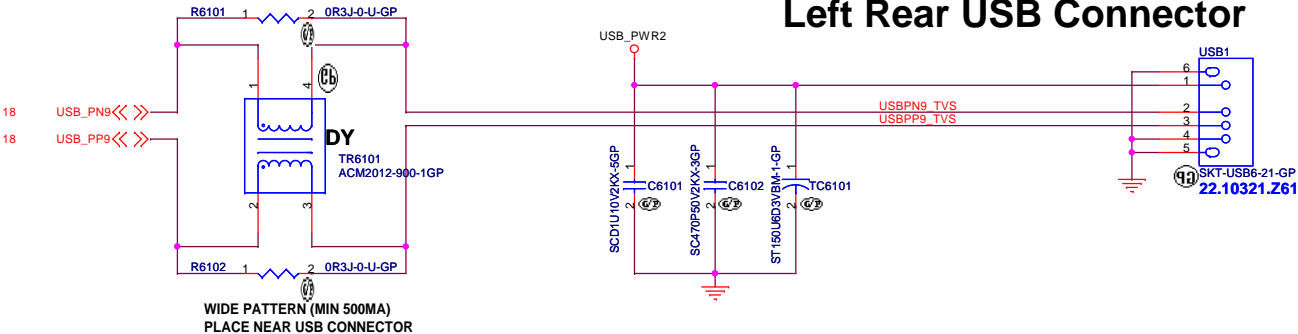
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Title			
Audio Jack			
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<Core Design>		
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
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Size	Document Number	Rev
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USB Connector

WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR



WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR

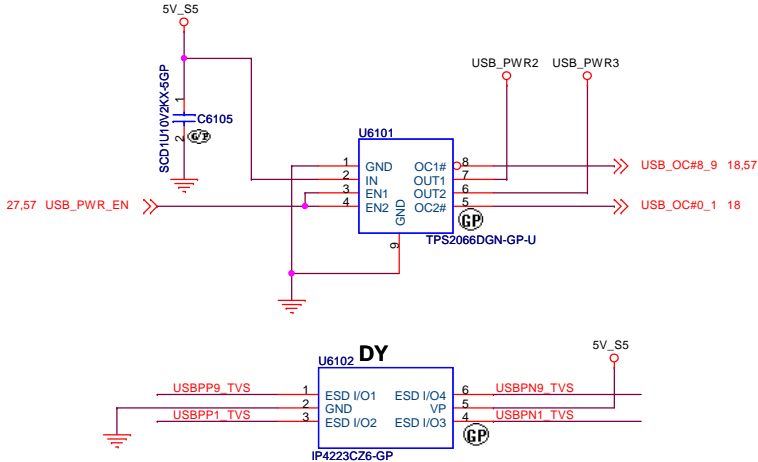
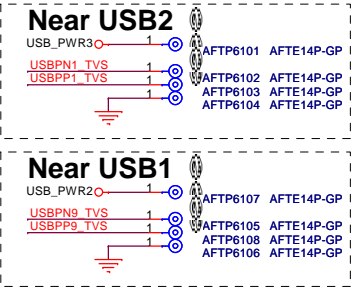
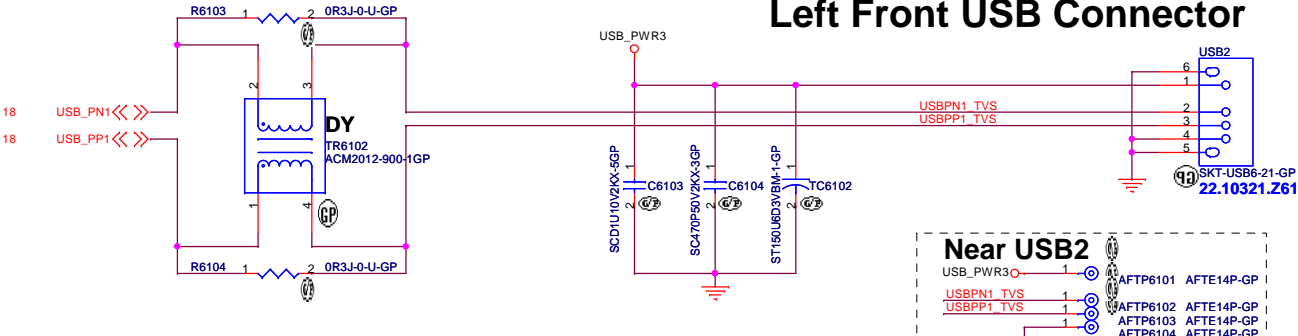


Table 61.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2066DGN	41R0511AA	74.02066.A71
TI	TPS2066DGN-1	N/A	74.02066.B71

Table 61.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Connector**

Size A3 Document Number: **LLW-1 / LGG-1** Rev: **-1**

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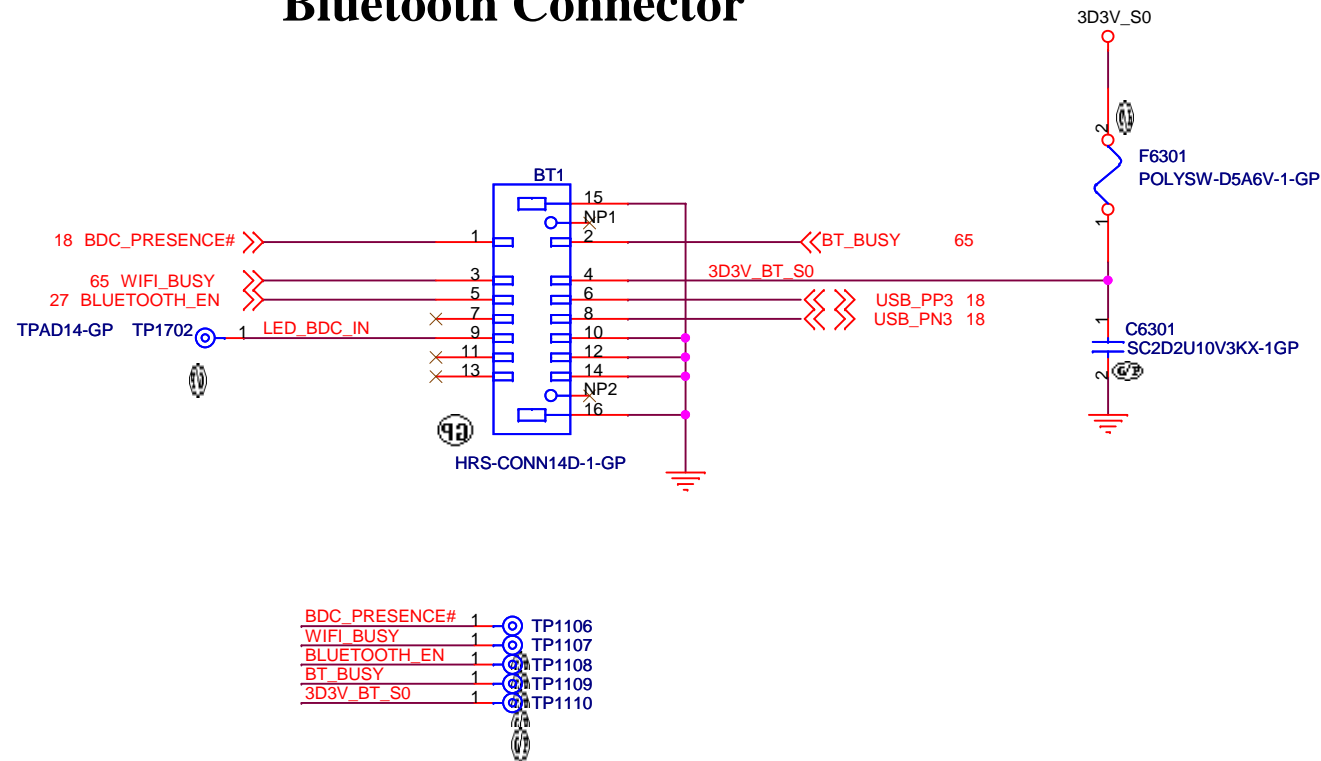
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Bluetooth Connector



<Core Design>

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Bluetooth			
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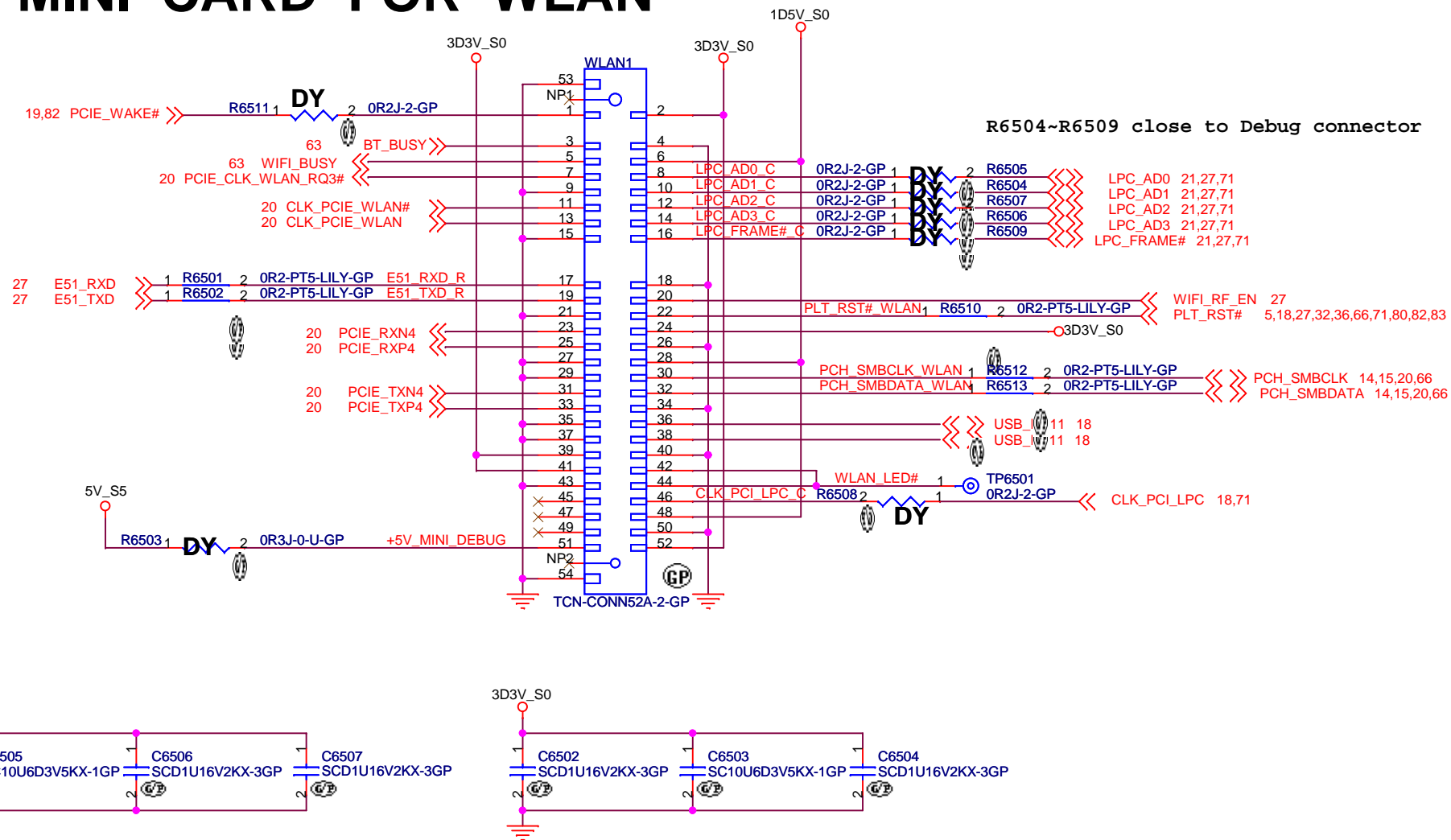
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Title <div>FingerPrint</div>		
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HALF MINI CARD FOR WLAN



<Core Design>

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

MINI CARD SLOT 1

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www.vinafix.vn

TC601 ST220U6D3VDM-20GP C601 SCD047U16V2KX-1-GP C602 SCD047U16V2KX-1-GP C603 SC33P50V2JN-3GP C604 SC33P50V2JN-3GP

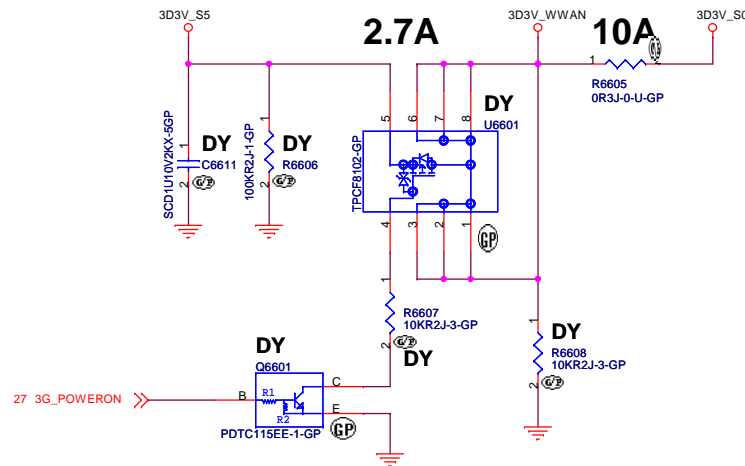
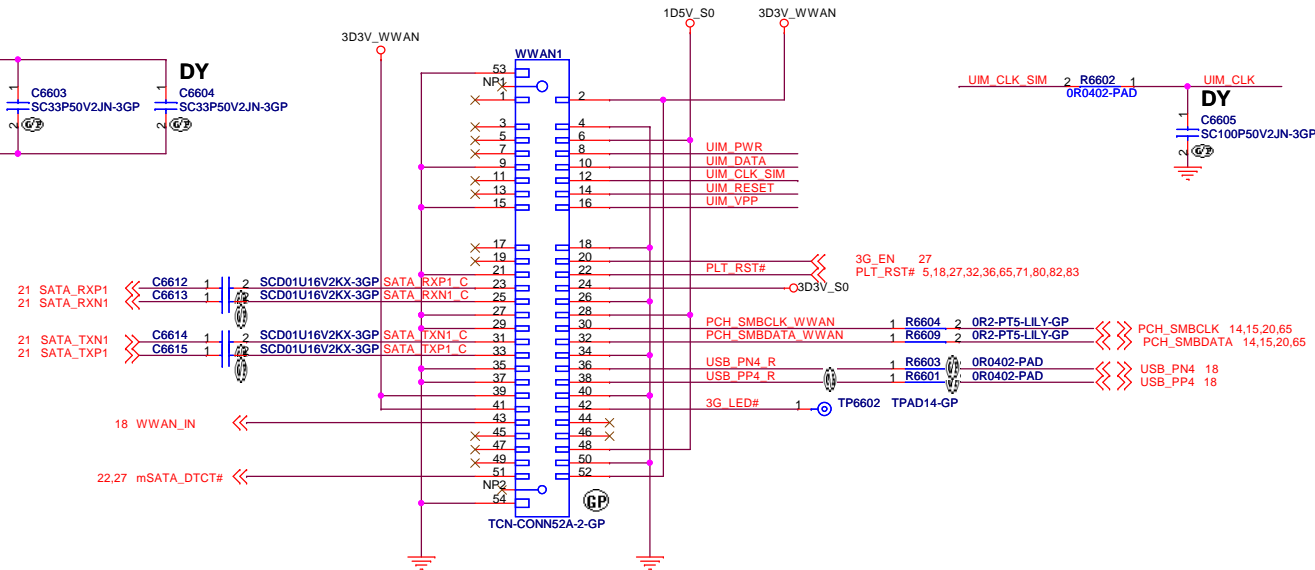
10V VCC

10kΩ RL

Vout

The top diagram shows the placement of capacitors C6606 and C6607 near Pin 24. C6606 is connected to Pin 24 and ground. C6607 is connected to Pin 24 and the 1D5V_S0 supply.

The bottom diagram shows the placement of capacitors C6608, C6609, and C6610 near Pin 25. C6608 is connected to Pin 25 and ground. C6609 is connected to Pin 25 and the 3D3V_S0 supply. C6610 is connected to Pin 25 and the 1D5V_S0 supply.



UIM_PWR

UIM_RESET

UIM_CLK

UIM_VPP

UIM_DATA

CD

NP1

NP2

C6616

DY

TP6601

SIM1

CARD-PUSH-7P-2-GP

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MINI CARD SLOT 2

LLW-1 / LGG-1

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Touch Pad Connector

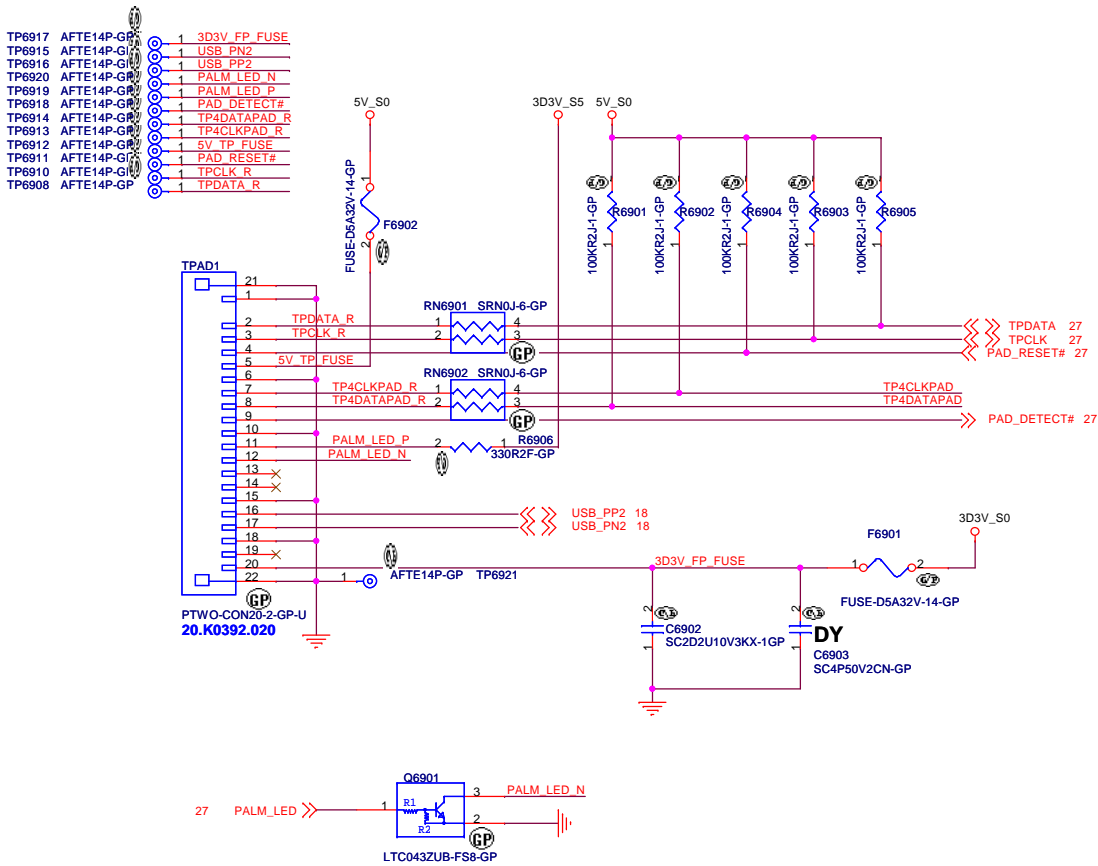
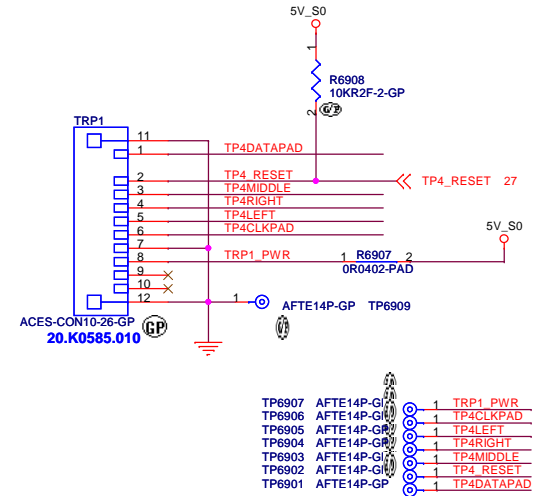


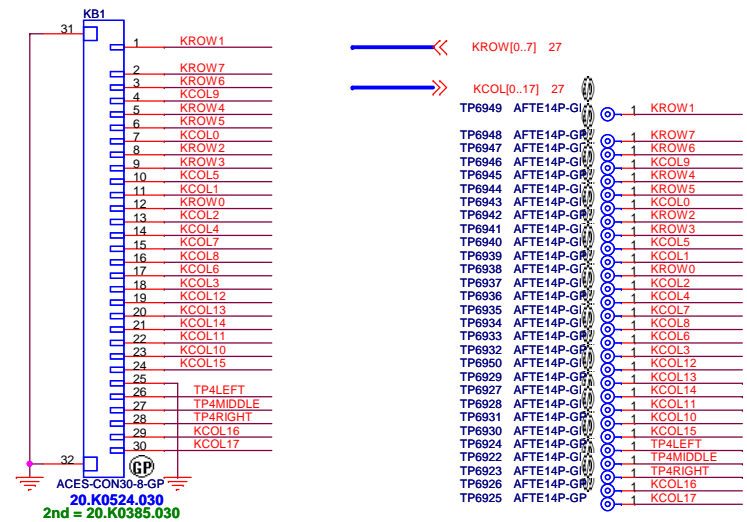
Table 69.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC143ZU	N/A	84.00143.E1K
ROHM	LTC043ZUB	N/A	84.00043.011
Panasonic	DRC5143Z0L	N/A	84.05143.011

Track Point Connector



KeyBoard Connector



<Core Design>

緯創資通

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Title

TOUCH PAD CONNECTOR

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LLW-1 / LGG-1

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-1

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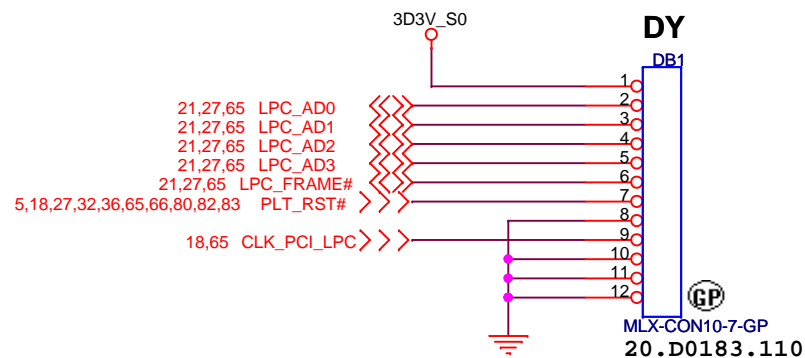
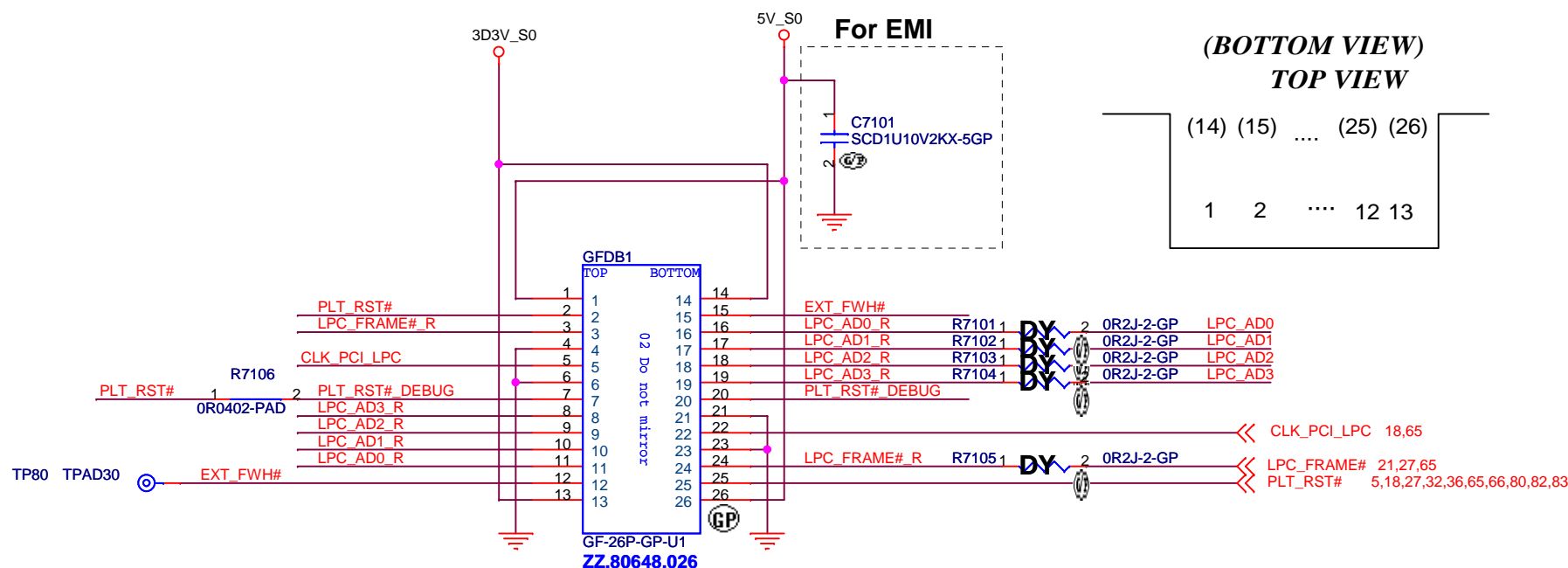
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Golden Finger for Debug Board



<Core Design>

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Title **DEBUG CONN**

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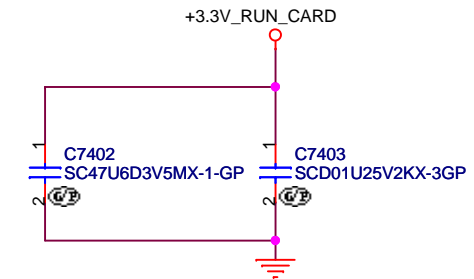
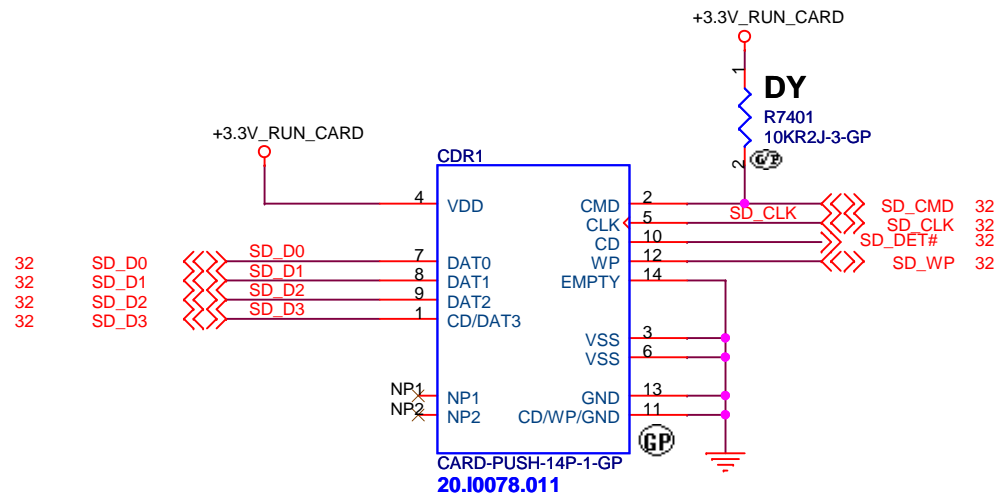
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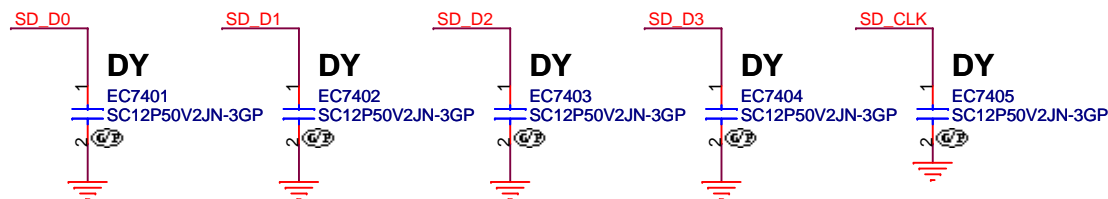
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Please apply Shield GND for SD_CLK signal between
R5U220 and SD Card Slot to decrease external noise.

Card Reader Connector



+3.3V_RUN_CARD trace = 40mil
C7402 lose CDR1



<Core Design>

緯創資通

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Title

CARD Reader CONN

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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Core Design>

緯創資通

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Title

New Card

Size
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<Core Design>

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<Core Design>

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Title			
TPM			
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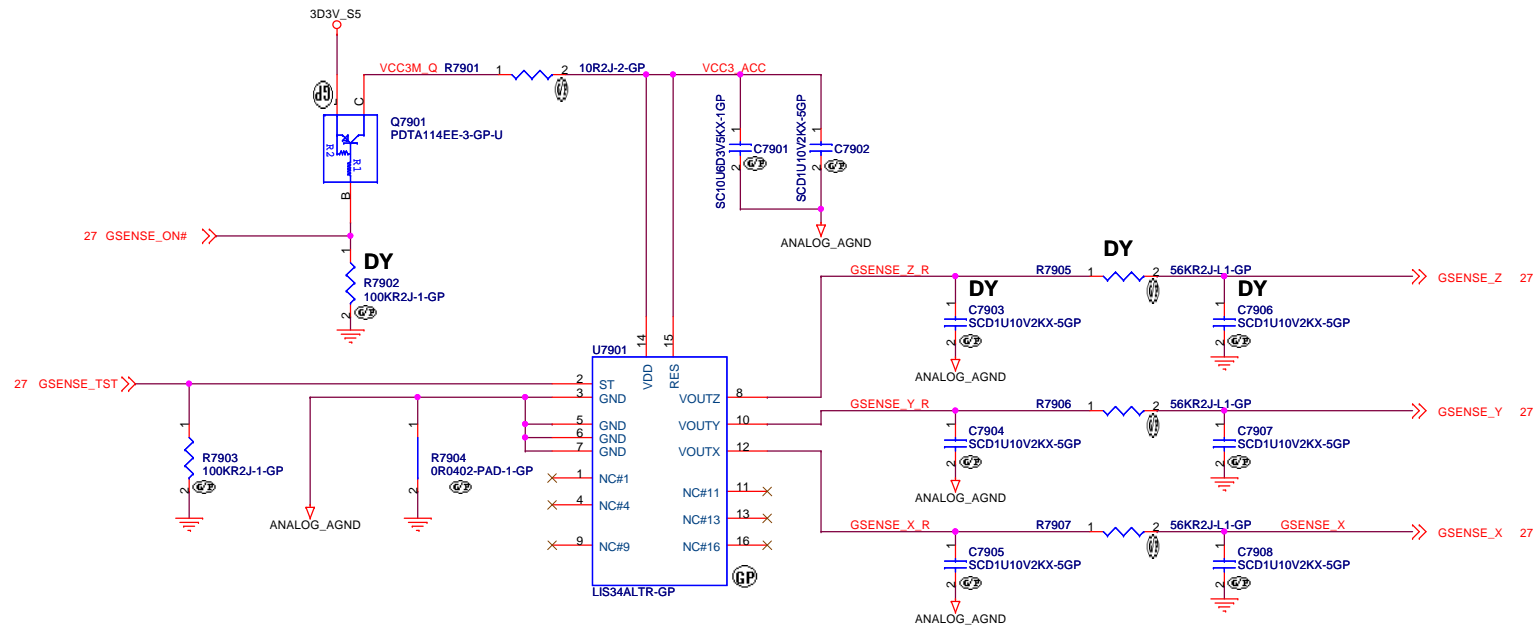
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G-Sensor



	LIS34AL KXTC8-2850	No Accel
R7902	NO_ASM	ASM
R7903	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C7904, C7905, Q7901, R7901, R7902, C7901, C7902, R7903, R508 close to U7901.

(2) Avoid routing under DCDC switching area.

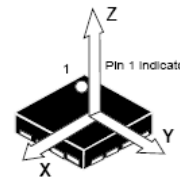


Table 79.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTA114EE	N/A	84.00114.H1K
ON	DTA114EET1G	N/A	84.DT114.B11
ROHM	LTA014EEB	N/A	84.00014.01H
Panasonic	DRA9114E0L	N/A	84.09114.A11

Table 79.2- Accelerometer multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ST	LIS34ALTR-GP	41R0828AA	74.00034.0BZ
ROHM-KIONIX	KXTC8-2850-GP	N/A	74.KXTC8.0BZ

<Core Design>

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Title	G-Sensor		
Size	Document Number	Rev	
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RFID

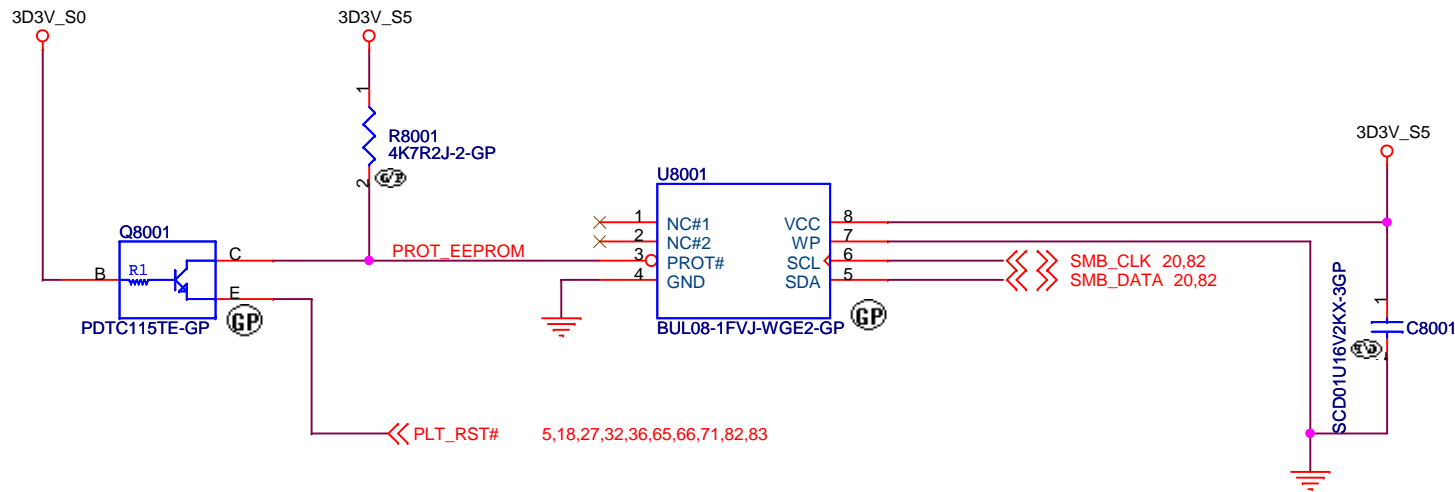



Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015EEB	N/A	84.00015.01H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
RFID	
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<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

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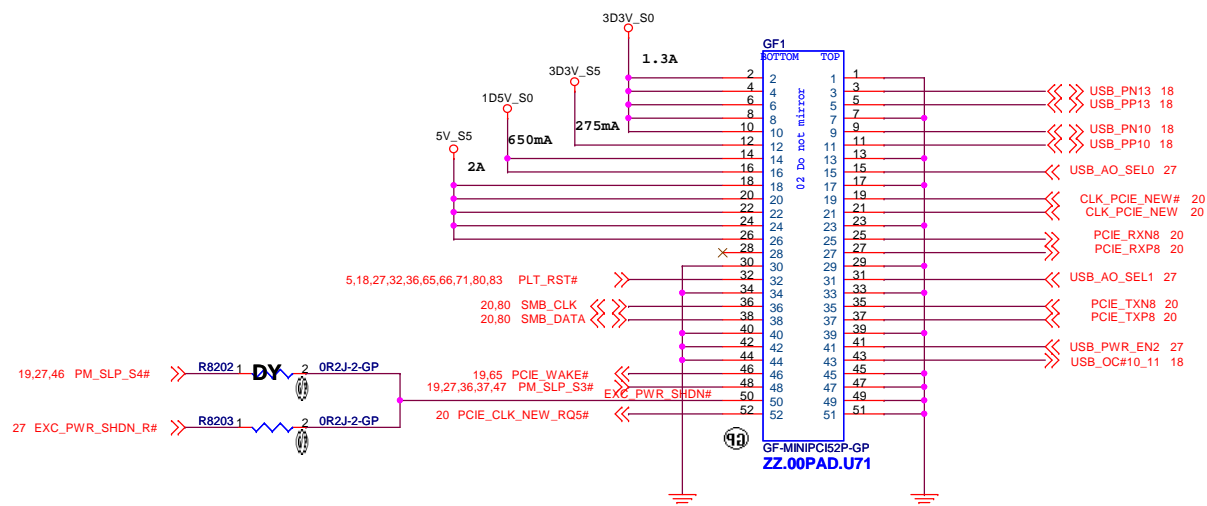
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LLW-1 / LGG-1

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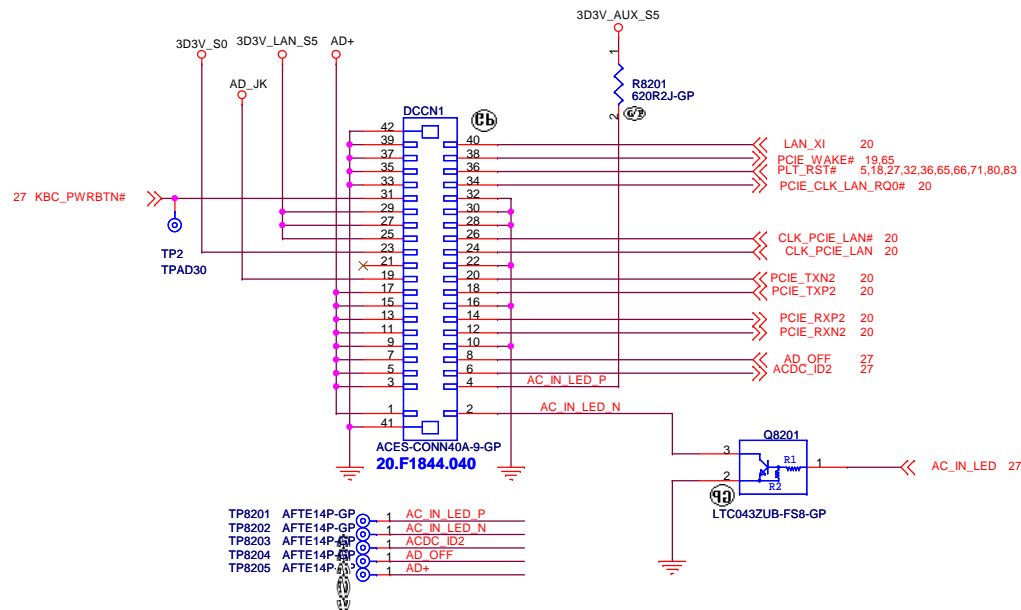
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TO EXP BOARD CONN



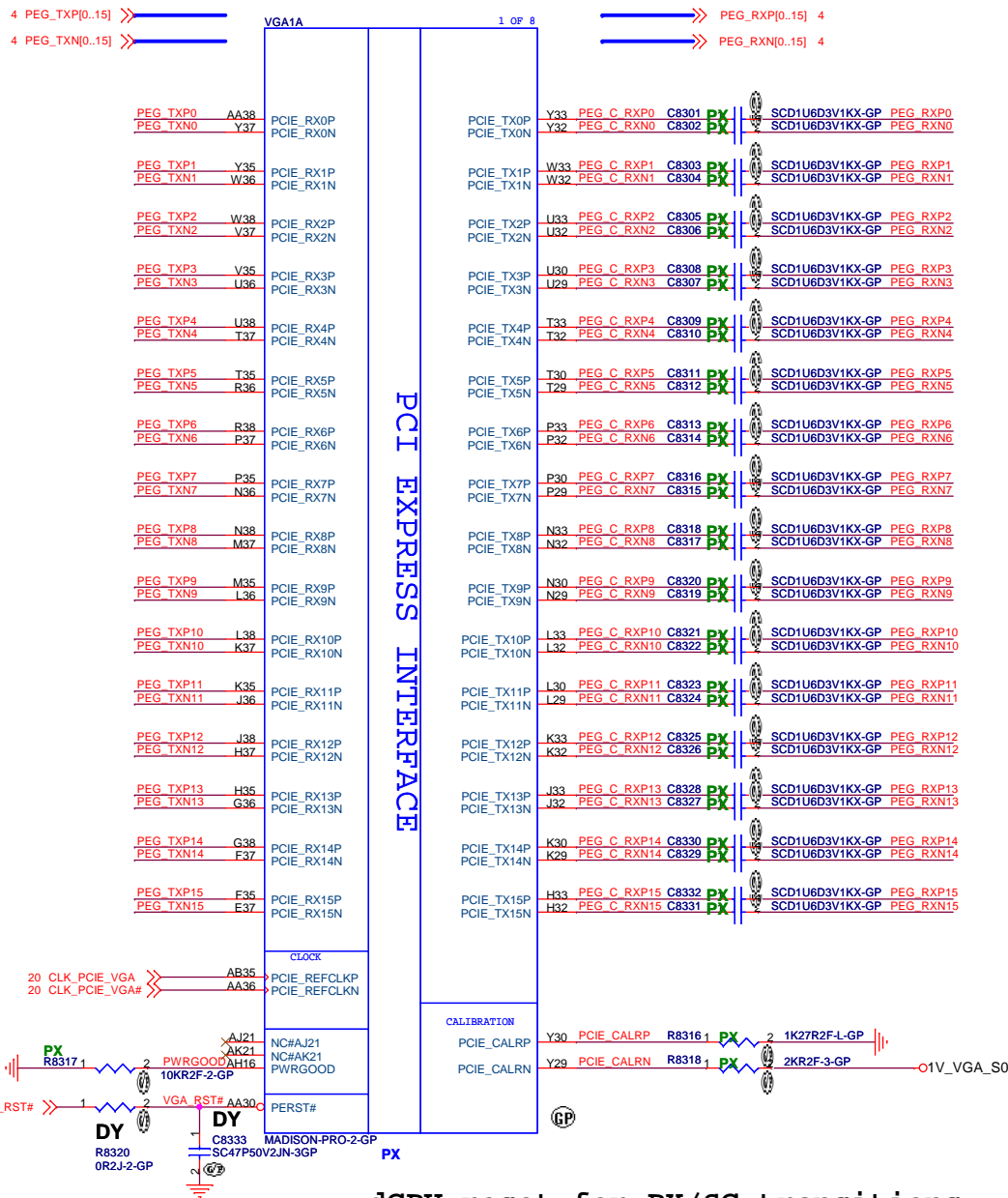
DC BOARD CONN



<Core Design>

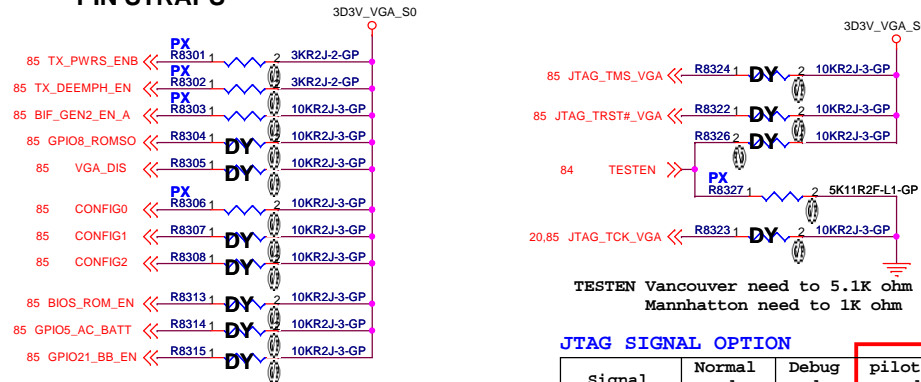
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			IO Board Connector	
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CONFIGURATION STRAPS				RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				0= DO NOT INSTALL RESISTOR 1= INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1	
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1	
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0	
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0	
GPIO8_ROMSO	GPIO8	RESERVED	0	0	
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0	
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)	
GPIO21_BB_EN	GPIO21	RESERVED	0	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0	
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0	
RSVD	H2SYNC	RESERVED	0	0	
RSVD	GENERICC	RESERVED	0	0	
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1	
AUD[0]	VSYSN		X	1	

PIN STRAPS



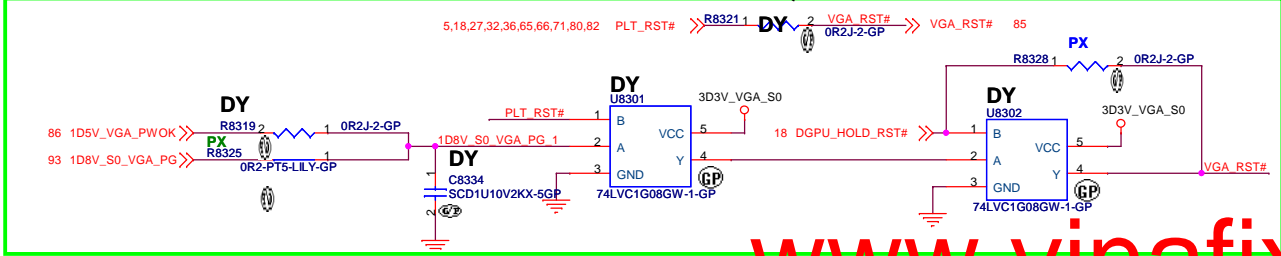
TESTEN Vancouver need to 5.1K ohm
Mannhattan need to 1K ohm

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC

	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACC	H

dGPU reset for PX/SG transitions



<Core Design>

緯創資通 Wistron Corporation
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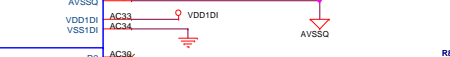
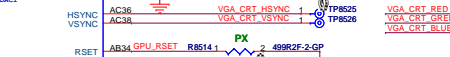
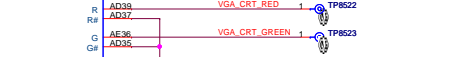
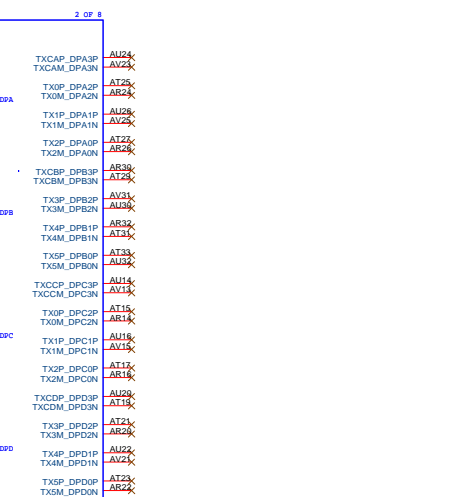
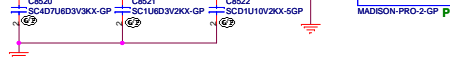
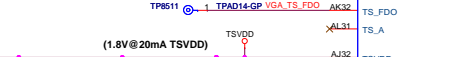
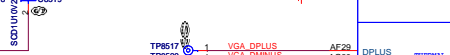
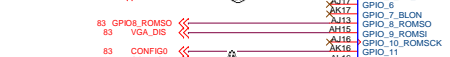
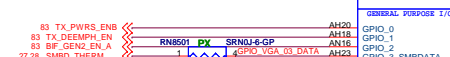
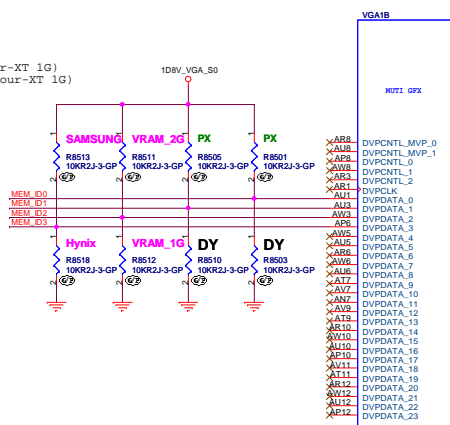
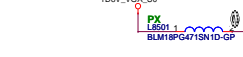
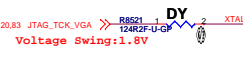
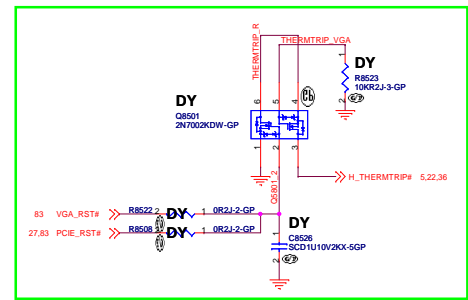
Title: **GPU PCIE/STRAPPING(1/5)**

Size A3 Document Number: **LLW-1 / LGG-1** Rev: **-1**

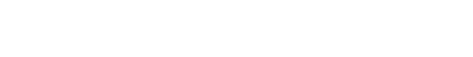
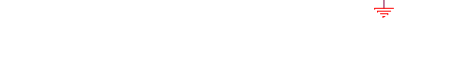
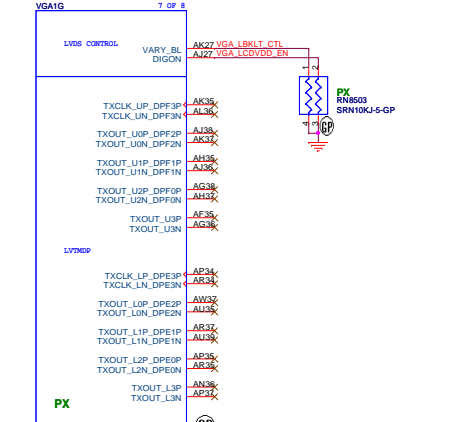
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DVPPDATA [3:2:1:0] for VRAM type
selection B/W strap
Should provide VRAM Table for VBIOS request

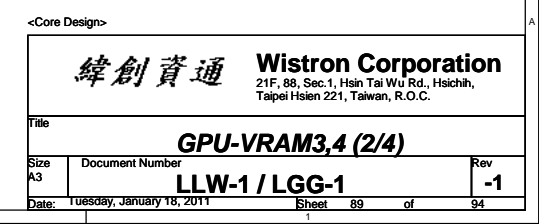
DVPPDATA [3:0]
0111 2Gbit Hynix-H5TQ2G63BFR-12C (800MHz) (Whistler-LP 2G / Seymour-XT 1G)
1111 2Gbit Samsung-K4W2G1646C-HC12 (800MHz) (Whistler-LP 2G / Seymour-XT 1G)
0011 1Gbit Hynix-H5TQ1G63BFR-12C (800MHz) (Whistler-LP 2G)
1011 1Gbit Samsung-K4W1G1646E-HC12 (800MHz) (Whistler-LP 1G)



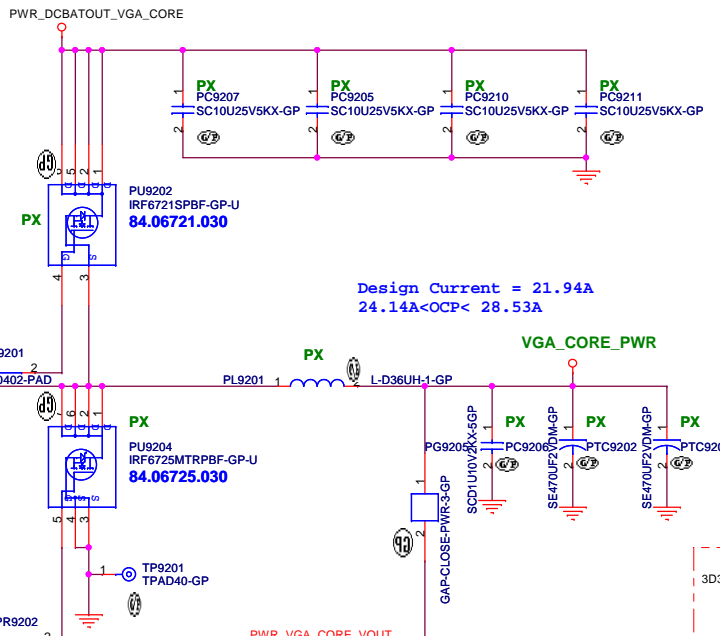
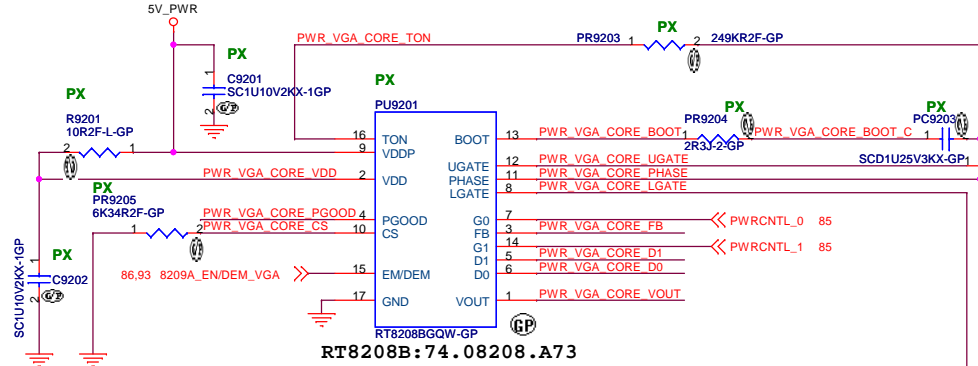
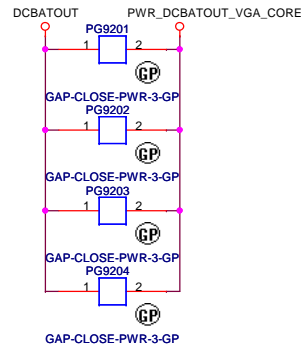
LVDS Interface



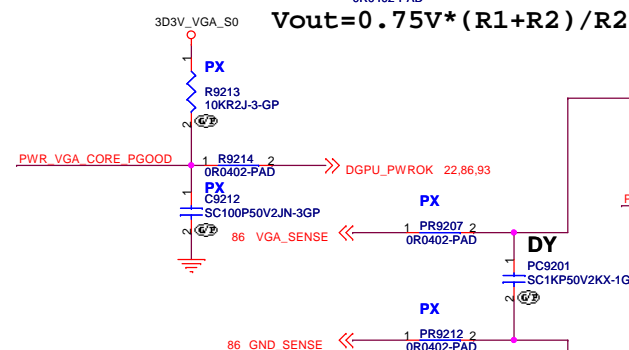
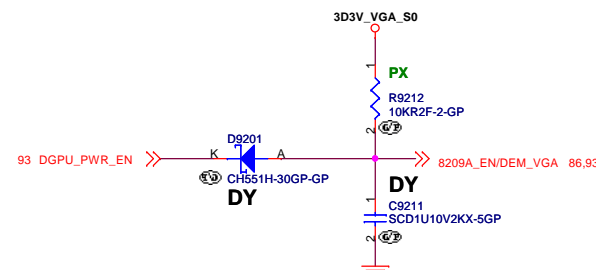
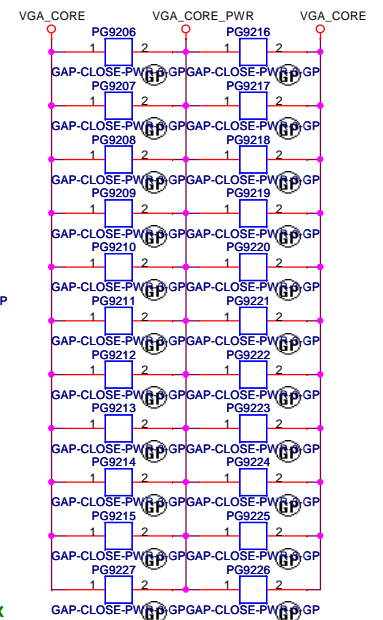
Clock Input Configuration - GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)



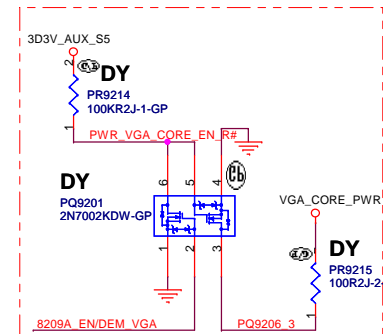
SSID = PWR.Plane.Regulator_GFX



Design Current = 21.94A
24.14A < OCP < 28.53A



$$V_{out} = 0.75V * (R1 + R2) / R2$$



MADSION PRO

Setting Vref Vout & Rfb-Top	Vref (V)	R9208	R9210	R9211	R9209
VOUT (Target)	VOUT (compute)	10K	50K	50K	75K
1.150	1.150			VID1	VID0
1.050	1.050			0	0
1.000	1.000			0	1
0.900	0.900			1	0
				1	1

WHIST => R9211 NO_ASM.
SEYMR => whole ASM

NVDD_ALT1	NVDD_ALT0	+VGA_CORE
H	L	1.12V or 1V
H	H	0.9V
		OUT= (R9208+R9210)/R9210

<Core Design>

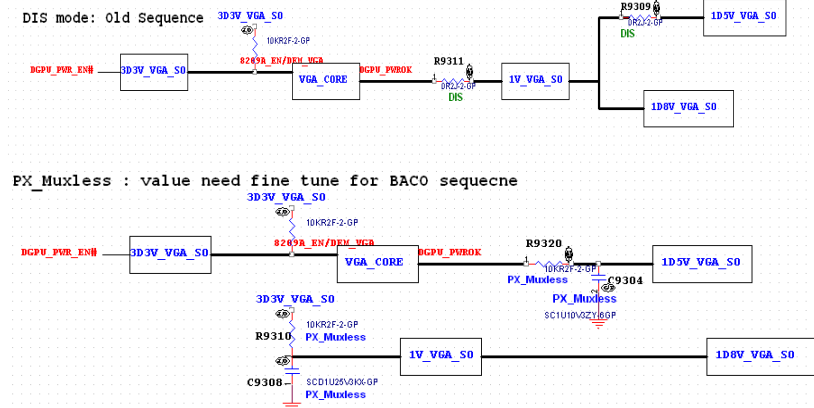
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title RT8208B +VGA CORE

Size A3 Document Number LLW-1 / LGG-1 Rev -1

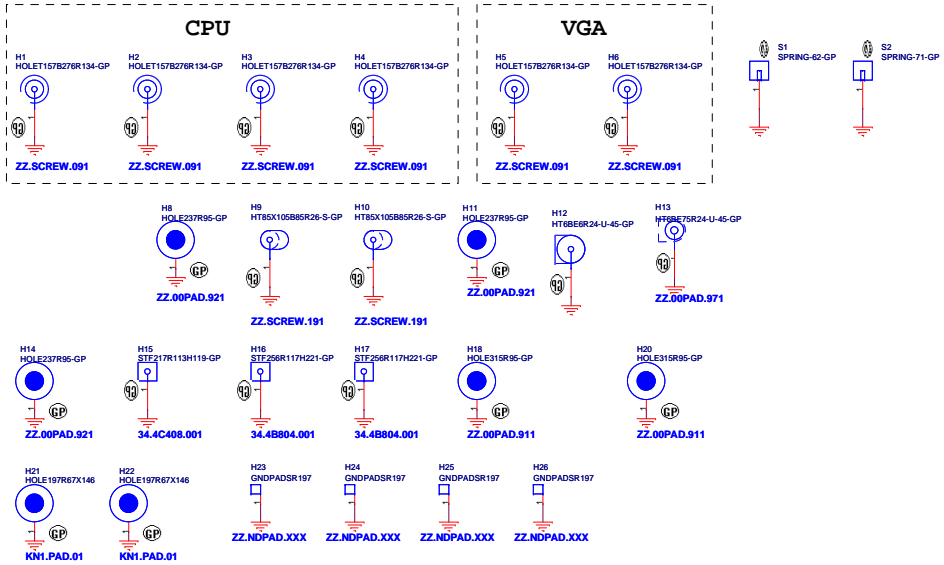
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1D5V_VGA_S0



Iomax=1A
OCP>1.35A





EMI CAP

